COE 202, Term 162

Digital Logic Design

HW# 3

Q.1. For the Boolean function E and F, as given in the following truth table:

X	Y	Z	E	F
0	0	0	1	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	0	1

(i) List the minterms and the maxterms of each function.

(ii) List the minterms of E' and F'.

(iii) List the minterms of E + F and E . F.

(iv) Express E and F in sum-of-minterms algebraic form.

(v) Simplify E and F to expressions with a minimum number of literals.

Q.2. Simplify the following Boolean functions **F** together with the don`t care conditions **d**. Find all prime implicants and essential prime implicants, and apply the selection rule.

(i) $F(A, B, C)=\Sigma\, m(3, 5, 6)$, $d(A,B,C)=\Sigma\, m(0, 7)$

(ii) $F(A, B, C, D)=\Sigma\, m(4, 6, 7, 8, 12, 15)$, $d(A, B, C, D)=\Sigma\, m(2, 3, 5, 10, 11, 14)$

(iii) $F(A, B, C, D) =)=\Pi\, M(1, 3, 5, 6, 7, 9, 10, 11, 14)$

Q.3. Simplify the following Boolean functions **F** together with the don`t care conditions **d** in (1) sum-of-products and (2) product-of-sums form:

(i) $F(W, X, Y, Z)=\Sigma\, m(0, 1, 2, 3, 7, 8, 10)$, $d(W, X, Y, Z)=\Sigma\, m(5, 6, 11, 15)$

(ii) $F(A, B, C, D)=\Sigma\, m(3, 4, 13, 15)$, $d(A, B, C, D)=\Sigma\, m(1, 2, 5, 6, 8, 10, 12, 14)$

(iii) $F(A, B, C, D, E, F)=\Sigma\, m(6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$

Q.4. The following Boolean expression: BE + B`DE` is a simplified version of the expression: A`BE + BCDE + BC`D`E + A`B`DE` + B`C`DE`. Are there any don`t care conditions? If so, what are they?

Q.5. Simplify each of the following expressions, and implement them with (1) NAND gates, (2) NOR gates. Assume that both true and complement versions of the input variables are available.

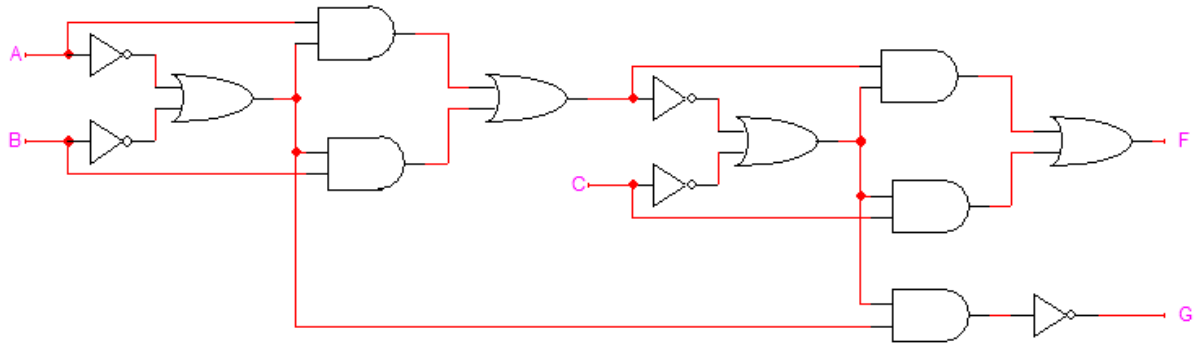
(i) WX` + WXZ + W`Y`Z` + W`XY` + WXZ`

(ii) XZ + XYZ` + WX`Y`

Q.6. Implement the following Boolean function with XOR and AND gates:

AB`C`D + A`BC`D + AB`CD` + A`BCD`

Q.7. Convert the AND/OR/NOT logic diagram shown below to (a) a NAND logic diagram, and (b) a NOR logic diagram.



Q.8. Derive the exclusive-OR/exclusive–NOR circuits for three-bit parity generator and a four-bit parity checker, using an even parity bit.

Q.9. A NAND gate with seven inputs is required. For each of the following cases, minimize the number of gates used in the multiple-level result:

(i) Design the 7-input NAND gate using 2-input NAND gates and NOT gates.

(ii) Design the 7-input NAND gate using 2-input NAND gates, 2-input NOR gates, and NOT gates.