KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 202 Digital Logic Design
Syllabus - Term 122

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuit analysis and design, multiplexers, decoders, adders. Sequential circuit analysis and design, basic flip-flops, clocking, and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. Machine-level programming.

Prerequisite: PHYS 102

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Office Hours S 9:00-10:00 UT 11:00-12:00 MW 1:00-2:00

Course Learning Outcomes

1. Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.
2. Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
3. Ability to use CAD tools to simulate and verify logic circuits.

Textbook

Alan B. Marcovitz , *Introduction to Logic Design*, Third Edition, McGraw-Hill, 2010.

Grading Policy

Discussions	5%	
Assignments	10%	
Quizzes	10%	
Exam I	20%	(Thur. Feb. 28, 2013, 1:00 PM)
Exam II	25%	(Thur. April 18, 2013, 1:00 PM)
Final	30%	

- Attendance will be taken regularly. For each missed 3 classes, a penalty of 0.5 will be deducted.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 10%.
- No makeup will be made for missing Quizzes or Exams.

Course Topics

Week	Topic
1	• Introduction. Information Processing and representation. Digital vs. Analog quantities. • Weighted Number Systems. Decimal, Binary, Octal and Hexadecimal. • Arithmetic in Binary and Hex (addition, subtraction& Multiplication), Number base conversion (Dec to Bin, Oct, and Hex).
2	• BCD Codes: Excess-3 & other BCD codes, Parity Bits. • Binary logic and gates, Truth tables, Boolean Algebra, Basic identities. Principle of duality. • DeMorgan's Theorem. • Manipulation of Boolean expressions. • Gate Implementation of Boolean expressions
3	• Canonical and Standard forms, Minterms, Maxterms, Sum of products & Products of Sums. • 2-Level gate implementation (SOP, POS). • From Truth tables to Boolean Expressions. • Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4-5	• ***Map method of simplification***: 2, 3 and 4-variable maps. Implicants, Prime Implicants, Essential Prime Implicants. • POS simplification. • Don't care conditions and simplification. • **Universal gates (NAND, NOR)** • ***Implementation using Nand and NOR gates:*** 2-level & Multilevel implementation. • Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
6-7	• Combinational Circuit Design Procedure & Examples. • Code Converter. • BCD to 7-Segment Display Conversion. • Half and Full Adders. • Ripple Carry Adder design and ***Delay*** analysis of RCA • Signed Numbers: sign-magnitude, 1`s complement, and 2`s complement. • Signed Binary Arithmetic. (Addition and Subtraction). • Binary Adder-Subtractor. • Carry Look-ahead adder. • ***Delay*** analysis
8-9	• Decoders 2x4, 3x8, 4x16. Designing large decoders from smaller decoders. Function implementation using decoders. • Encoders: Priority Encoders. • Multiplexers**:** 2x1, 4x1. Constructing large MUXs from smaller ones. • Function implementation using multiplexers. • Magnitude Comparator • MSI Design Examples
10	• Sequential Circuits: Latches, Clocked latches: SR, D, T and JK. Race problem in clocked JK-Latch. • Flip-Flops: Master-Slave, D-FF.

	• Using D-FF to build other flip-flops.
11	• Asynchronous/Direct Clear and Set Inputs. Setup, Hold, FF propagation delay. • Sequential Circuit Design. Design procedure, State diagrams and state tables. • Analysis of Sequential Circuits. State table, State diagram.
12	• Mealy vs. Moore machine. • Design Examples and Calculation of maximum clock frequency.
13	• Registers, Registers with parallel load. • Synchronous Binary Counters*:* Up-Down Counters • Counters with Parallel load, enable, synchronous clear and asynchronous clear. • Use of available counters to build counters of different count. • Design with unused States • Shift Registers. Bi-directional shift register.
14	• Memory devices: RAMs & ROMs . • Combinational Circuit Implementation with ROM. • Sequential Circuit Implementation using ROMs. • Programmable Logic Devices: PLAs, PALs, FPGA’a.