May 6, 2006

COMPUTER ENGINEERING DEPARTMENT

COE 202

FUNDAMENTALS OF COMPUTER ENGINEERING

Major Exam II

Second Semester (052)

Time: 8:00-10:00 PM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Q5	20	
Total	100	

Dr. Aiman El-Maleh

[20 Points]

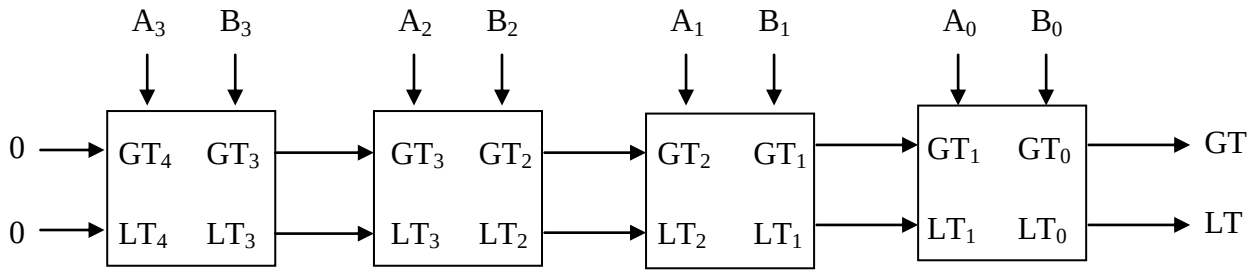
(Q1) Consider the Boolean function F(A, B, C, D)=Σ m(0, 3, 13, 14).

(i) Implement the function F using only 4x1 multiplexers and inverters.

(ii) Implement the function F using only 2x4 decoders, and 2-input OR gates. Assume that the decoders have enable input.

[20 Points]

(Q2) It is required to design a 4-bit comparator that compares two 4-bit numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$, and produces two outputs GT and LT. If A>B, then the output signal GT is set to 1 and LT is set to 0. If A<B, then the output signal LT is set to 1, and GT is set to 0. Otherwise both signals will be set to 0, which indicates that the two numbers are equal (i.e. A=B). The 4-bit comparator circuit can be designed in a modular way as shown below:



(i) Obtain the truth table for the 1-bit comparator bit-slice, where A_i and B_i are the two bits to be compared, GT_{i+1} and LT_{i+1} are the inputs from the outputs of the previous stage and GT_i and LT_i are the outputs of the current stage. Note that GT_i and LT_i signals propagate from the most significant bit to the least significant bit.

(ii) Show a minimized gate-level design for the 1-bit comparator bit-slice.

[20 Points]

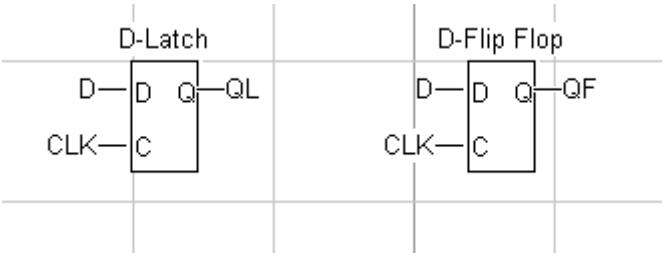
(Q3) It is required to design a circuit that has two 4-bit inputs $\mathbf{A=A_3A_2A_1A_0}$ and $\mathbf{B=B_3B_2B_1B_0}$ and one **6-bit output** $\mathbf{C= C_5C_4C_3C_2C_1C_0}$. The circuit implements the following eight functions based on the values of the three selection inputs S2, S1 and S0.

S2 S1 S0	Function
0 0 0	C=A + B
0 0 1	C=A - B
0 1 0	C=A+1
0 1 1	C=A-1
1 0 0	C=B
1 0 1	C=-B
1 1 0	C=2B
1 1 1	C=3B

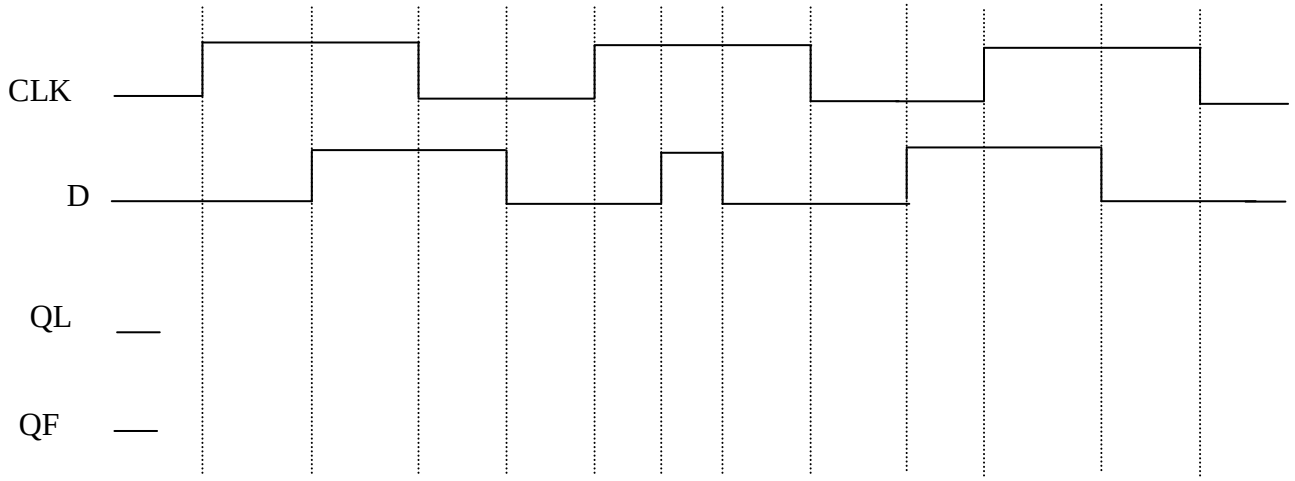
Assume that you can use MSI components like Adder, Multiplexor, Decoder in your design as needed. Note that you only need to show the used components as blocks showing only their inputs and outputs without showing their detailed implementations.

[20 Points]

(Q4) Given the D-latch and the rising edge-triggered D-flip flop shown below:



(i) Complete the timing diagram given below:



(ii) Show an implementation of the D-latch using only NAND gates and inverters.

(iii) Show an implementation of the rising-edge triggered D-flip flop using D-latches and inverters.

[20 Points]

(Q5) A sequential circuit has two JK flip-flops A and B, input X and one output Z. The flip-flop input equations and output function are:

$J_A = B\ X$ $K_A = B$ $Z = A\ X\ B`$

$J_B = X$ $K_B = X`$

(i) Draw the logic diagram of the circuit.

(ii) Obtain the **state table** of the circuit.

(iii) Obtain the **state diagram** of the circuit.

(iv) Is the circuit a **Mealy** or **Moore** model?

(v) Is the input sequence {0, 0} a **synchronizing** sequence for the circuit? If the answer is yes, what will be the state reached after synchronization.