KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

Term 132 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U 26/1 | Syllabus & Course Introduction. Information Processing and representation. Digital vs. Analog quantities. Digitization of Analog signals. Minimizing Quantization Error, Digital representation of information. |  |
| 2 | T 28/1 | Effect of noise on the reliability and choice of digital system, Maximizing Noise Margin. Numbering Systems, Weighted Number Systems, the Radix, Radix Point. Binary, Octal and Hexadecimal systems. | Chapter 1 |
| 3 | TH 30/1 | Important Properties. Number Base Conversion, Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Converting Fractions. | Chapter 1 |
| 4 | U 2/2 | Binary and Hexadecimal Addition, Subtraction, Binary and Hexadecimal Multiplication. Binary Codes for Decimal Digits. | Chapter 1 |
| 5 | T 4/2 | Binary Codes for Decimal Digits, Character Storage, ASCII Code. Error Detection, Parity Bit. | Chapter 1 |
| 6 | TH 6/2 | Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations. Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra. | 2.2-2.4 |
| 7 | U 9/2 | Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra, Algebraic Manipulation. **(Quiz#1)** | 2.2-2.4 & 2.7 |
| 8 | T 11/2 | Algebraic Manipulation. | 2.7 |
| 9 | TH 13/2 | Minterms, Expressing Functions as a Sum of Minterms, Maxterms. Canonical Forms. | 2.5 |
| 10 | U 16/2 | Maxterms, Expressing Functions as a Product of Maxterms. | 2.5 |
| 11 | T 18/2 | Standard Forms, Two-Level Implementations of Standard Forms. Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. Propagation Delay. | 2.5 |
| 12 | TH 20/2 | Propagation Delay, Timing Diagrams. Fanin Limitations, Fanout Limitations. |  |
| 13 | U 23/2 | Fanin Limitations, Fanout Limitations, Use of High- Drive Buffers, Use of Multiple Drivers. Gates with Tri-State Outputs. |  |
| 14 | T 25/2 | ***Map method of simplification***: Two-, and Three-variable K-Map. **(Quiz#2)** | 3.1 |
| 15 | TH 27/2 | Major Exam I Review. |  |
|  | S 1/3 | **Major Exam I** |  |
| 16 | U 2/3 | ***Map method of simplification***: Three-variable K-Map. | 3.1-3.2 |
| 17 | T 4/3 | ***Map method of simplification***: Four-variable K-Map. Implicants, Prime Implicants. Essential Prime Implicants. Simplification procedure. | 3.4 |
| 18 | TH 6/3 | Simplification procedure. POS simplification. | 3.3-3.5 |
|  | TH 6/3 | **Last Day for Dropping with W** |  |
| 19 | U 9/3 | Don’t Care Conditions, Simplification procedure using Don’t Cares, Five-variable K-map simplification. Six-variable K-map simplification. | 3.3-3.5 |
| 20 | T 11/3 | types of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate, universal gates, Two-Level Implementation using Nand/Nor gates. General circuit implementations using NAND/Nor gates, Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. | 2.6, 2.8 |
| 21 | TH 13/3 | Properties of XOR/XNOR Operations, XOR/XNOR for >2 Variables. The Odd & Even Functions, Parity Generation and Checking. Combinational Logic Circuits, Combinational Circuits Design Procedure. BCD to 7-Segment Decoder for LED. Hierarchical Design, Iterative Arithmetic Combinational Circuits. Adder Design. | 2.1 & 5.1 |
| 22 | U 16/3 | Hierarchical Design, Iterative Arithmetic Combinational Circuits, Iterative equal and magnitude comparator design. (**Introduction to LogicWorks**). | 5.1 |
| 23 | T 18/3 | Half Adder, Full Adder, 4-bit Ripple Carry Adder. **(Quiz#3)** | 5.1 |
| 24 | TH 20/3 | No Class. |  |
|  | 23-29/3 | **Midterm Vacation** |  |
| 25 | U 30/3 | 4-bit RCA: Carry Propagation & Delay, Carry Look-ahead Adder, Delay for the 4-bit CLA Adder. | 5.1 |
| 26 | T 1/4 | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. | 1.2.3-1.24 & 5.1.2-5.1.3 |
| 27 | TH 3/4 | 2’s complement representation, addition and subtraction, overflow detection, sign extension. | 1.2.3-1.24 & 5.1.2-5.1.3 |
|  | TH 3/4 (Makeup) | Adder/Subtractor for Signed 2’s Complement.. BCD Adder. Binary Multiplier. | 1.2.3-1.24 & 5.1.2-5.1.3 & 5.8 |
| 28 | U 6/4 | Enabling Function, Decoders. Implementing Functions using Decoders. Hierarchical design of decoders. | 5.2-5.4 |
| 29 | T 8/4 | **Encoders**: Priority Encoders. **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones. Function implementation using multiplexers. | 5.2-5.4 |
| 30 | TH 10/4 | Function implementation using multiplexers.  Applications of encoders, decoders and Multiplexers. | 5.4 |
|  | TH 10/4 | **Last Day for Dropping all Courses with W** |  |
| 31 | U 13/4 | Demultiplexer, Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Selecting the larger of two 4-bit numbers. | 5.4 & 5.8 |
| 32 | T 15/4 | Absolute Value of a number. multiplication and division by a constant. BCD to Excess-3 Code Converter using a decoder and straight binary encoder. Introduction to Sequential Circuits, NOR Set–Reset (SR) Latch. | 5.8 & 6.1-6.3 |
| 33 | TH 17/4 | (**Quiz#4**) Major Exam II Review. |  |
|  | S 19/4 | **Major Exam II** |  |
| 34 | U 20/4 | NOR Set–Reset (SR) Latch. NAND Set–Reset (SR) Latch, Clocked (or controlled) SR NAND Latch, D Latch. Timing Problem of the transparent Latch. Types of sequential circuits: Synchronous vs. Asynchronous. | 6.1-6.3 |
| 35 | T 22/4 | Flip flops, Edge-Triggered D-type Flip-Flop.  Synchronous and asynchronous reset. | 6.1-6.3 |
| 36 | TH 24/4 | Other types of FFs: SR, JK and T flip-flops. Characteristic table, Characteristic equation, Excitation table, Designing flip-flops using other flip-flops. | 6.1-6.3 |
| 37 | U 27/4 | Sequential Circuit Analysis: One-Dimensional State Table. Two-Dimensional State Table, Sate Diagram. Moore and Mealy Models. Initializing sequence. | 6.4 |
| 38 | T 29/4 | Analysis of sequential circuit (moore model). Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. Sequential Circuit Design Procedure, Serial Adder Design, 2’s complement, sequence detector. | 6.4 & 7.4 |
| 39 | TH 1/5 | Sequential circuit design and implementation examples: Sequential Comparator, Sequence Detectors (Moore). Two-sequences detector, sequential 3\*X circuit. | 7.4 |
| 40 | U 4/5 | Sequential Circuit Design Examples: Sequential Comparator, BCD-to-excess-3 code conversion, Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers. | 7.4 & 8.1 |
| 41 | T 6/5 | Shift Register Applications. Linear Feedback Shift Register (LFSR). (**Quiz#5**) | 8.1 |
| 42 | TH 8/5 | Designing Synchronous Counters using FSMs, Ripple Counter, Up-Down Synchronous Counter with Enable & Parallel Load. Synchronous Counters. Building Large counters from Small counters. Modulo counters. Counters as Frequency Dividers. | 8.2 |
|  | TH 8/5 | **Dropping all Courses with WP/WF** |  |
| 43 | U 11/5 | Counters as Frequency Dividers. Programmable Implementation Technologies: Overview, Why Programmable Logic? Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM). | 8.2 & 5.6 |
| 44 | T 13/5 | Read Only Memory (ROM), Logic implementation using ROMs. Sequential Circuit implementation using ROMs. Programmable Array Logic (PAL), Programmable Logic Array (PLA). | 5.6 |
| 45 | TH 15/5 | Programmable Logic Array (PLA). Review. | 5.6 |