KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

Term 122 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | S 26/1 | Syllabus & Course Introduction. Information Processing and representation. Digital vs. Analog quantities. Digitization of Analog signals. |  |
| 2 | M 28/1 | Digital representation of information, Effect of noise on the reliability and choice of digital system. Numbering Systems, Weighted Number Systems, the Radix, Radix Point. | Chapter 1 |
| 3 | W 30/1 | Binary, Octal and Hexadecimal systems, Conversion between binary, Octal and Hexadecimal, Important Properties. | Chapter 1 |
| 4 | S 2/2 | Important Properties. Number Base Conversion, Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Converting Fractions. | Chapter 1 |
| 5 | M 4/2 | Converting Fractions, Binary Addition, Subtraction, Multiplication, Hexadecimal Addition and Subtraction, Binary Codes for Decimal Digits. | Chapter 1 |
| 6 | W 6/2 | Binary Codes for Decimal Digits, Character Storage, ASCII Code. Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations. | Chapter 1 & 2.2 |
| 7 | S 9/2 | Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra, Algebraic Manipulation. | 2.2-2.4 & 2.7 |
| 8 | M 11/2 | Algebraic Manipulation **(Quiz#1)** | 2.7 |
| 9 | W 13/2 | Algebraic Manipulation, MinTerms, Expressing Functions as a Sum of Minterms. | 2.7 & 2.5 |
| 10 | S 16/2 | MaxTerms, Expressing Functions as a Product of Maxterms. Operations on functions performed as operations on Minterms. Canonical Forms, Standard Forms. | 2.5 |
| 11 | M 18/2 | Two-Level Implementations of Standard Forms. Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. Propagation Delay, Timing Diagrams. | 2.5 |
| 12 | W 20/2 | Fanin Limitations, Fanout Limitations, Use of High- Drive Buffers, Use of Multiple Drivers, Gates with Tri-State Outputs. |  |
| 13 | S 23/2 | ***Map method of simplification***: Two-, and Three-variable K-Map. (**Quiz#2**) | 3.1 |
| 14 | M 25/2 | ***Map method of simplification***: Three-variable & Four-variable K-Map. Implicants, Prime Implicants, Essential Prime Implicants. Simplification procedure | 3.1-3.2 |
| 15 | W 27/2 | Simplification procedure, POS simplification | 3.4 |
|  | Th. 28/2 | **Major Exam I** |  |
| 16 | S 2/3 | SOP Simplification procedure using Don’t Cares, Five-variable K-map simplification. | 3.3-3.5 |
| 17 | M 4/3 | Six-variable K-map simplification, types of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate, universal gates, Two-Level Implementation using Nand/Nor gates. | 3.5, 2.6 |
| 18 | W 6/3 | Solution of Major Exam I |  |
|  | W 6/3 | **Last Day for Dropping with W** |  |
| 19 | S 9/3 | General circuit implementations using NAND/Nor gates, Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. Properties of XOR/XNOR Operations, XOR/XNOR for >2 Variables. The Odd & Even Functions, Parity Generation and Checking. | 2.6, 2.8 |
| 20 | M 11/3 | (**Quiz#3**) |  |
| 21 | W 13/3 | Combinational Logic Circuits, Combinational Circuits Design Procedure. BCD to Excess 3 Code Converter. BCD to 7-Segment Decoder for LED. (Introduction to LogicWorks) | 2.1 |
| 22 | S 16/3 | Hierarchical Design, Iterative Arithmetic Combinational Circuits, Iterative equal and magnitude comparator design, Adder Design. Half Adder, Full Adder, 4-bit Ripple Carry Adder. | 5.1 |
| 23 | M 18/3 | 4-bit RCA: Carry Propagation & Delay. Building a device Symbol in Logic Works. | 5.1 |
|  | M 18/3 (Makeup) | 4-bit RCA: Carry Propagation & Delay, Carry Lookahead Adder, Delay for the 4-bit CLA Adder. | 5.1 |
| 24 | W 20/3 | No Class |  |
|  | **23-27/3** | **Midterm Vacation** |  |
| 25 | S 30/3 | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. Adder/Subtractor for Signed 2’s Complement. | 1.2.3-1.24 & 5.1.2-5.1.3 |
| 26 | M 1/4 | Signed Number Representation. Overflow Detection. | 1.2.3-1.24 & 5.1.2-5.1.3 |
| 27 | W 3/4 | BCD Adder, Binary Multiplier. Enabling Function, Decoders. | 5.8 & 5.2 |
| 28 | S 6/4 | Decoders, Hierarchical design of decoders, Implementing Functions using Decoders. (Building a device Symbol in Logic Works). | 5.2 |
| 29 | M 8/4 | (**Quiz#4**) |  |
| 30 | W 10/4 | Hierarchical design of decoders, **Encoders**: Priority Encoders. **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones. | 5.2-5.4 |
|  | W 10/4 | **Last Day for Dropping all Courses with W** |  |
| 31 | S 13/4 | Constructing large MUXs from smaller ones.Function implementation using multiplexers. Demultiplexer. | 5.4 |
| 32 | M 15/4 | Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Selecting the larger of two 4-bit numbers, Absolute Value of a number. BCD to Excess-3 Code Converter using a decoder and straight binary encoder, Shifter Design, multiplication and division by a constant. | 5.8 |
| 33 | W 17/4 | Introduction to Sequential Circuits, Types of sequential circuits: Synchronous vs. Asynchronous, NOR Set–Reset (SR) Latch. NAND Set–Reset (SR) Latch, Clocked (or controlled) SR NAND Latch, D Latch. Timing Problem of the transparent Latch. | 6.1-6.3 |
|  | Th. 18/4 | **Major Exam II** |  |
| 34 | S 20/4 | Timing Problem of the transparent Latch, Flip flops, Edge-Triggered D-type Flip-Flop. Other types of FFs: SR, JK and T flip-flops. | 6.1-6.3 |
| 35 | M 22/4 | Other types of FFs: JK and T flip-flops. Characteristic table, Characteristic equation, Excitation table, Designing flip-flops using other flip-flops. | 6.1-6.3 |
| 36 | W 24/4 | Sequential Circuit Analysis: One-Dimensional State Table. Sequential Circuit Analysis: One-Dimensional State Table, Two-Dimensional State Table, Sate Diagram, Moore and Mealy Models. Synchronous & Asynchronous Reset. | 6.4 |
| 37 | S 27/4 | Sequential Circuit Analysis, Flip-Flop Timing Parameters: Setup and hold times. | 6.4 |
| 38 | M 29/4 | (**Quiz#5**) |  |
| 39 | W 1/5 | Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. Sequential Circuit Design Procedure, Serial Adder Design. | 7.1 & 7.4 |
| 40 | S 4/5 | Sequential circuit design examples: Sequential Comparator, Sequence Detectors (Mealy & Moore). | 7.4 |
| 41 | M 6/5 | Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers. Shift Register Applications. | 8.1 |
| 42 | W 8/5 | Designing Synchronous Counters using FSMs, Up-Down Ripple Counter with Enable & Parallel Load. Synchronous Counters. Modulo N counters. | 8.2 |
|  | W 8/5 | **Dropping all Courses with WP/WF** |  |
| 43 | S 11/5 | Modulo N counters, Building Large counters from Small counters, Counters as Frequency Dividers. | 8.2 |
| 44 | M 13/5 | Asynchronous (Ripple) Counter, Programmable Implementation Technologies: Overview, Why Programmable Logic? Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM), Types of ROM Devices, Read Only Memory (ROM) Advantages/Limitations. Logic implementation using ROMs. | 8.2 & 5.6 |
| 45 | W 15/5 | Logic implementation using ROMs. Programmable Array Logic (PAL), Programmable Logic Array (PLA). | 5.6 |