KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
*COMPUTER ENGINEERING DEPARTMENT*

COE 202 Digital Logic Design

 Term 121 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | S 1/9 | Syllabus & Course Introduction. |  |
| 2 | M 3/9 | Information Processing and representation. Digital vs. Analog quantities. Digitization of Analog signals. | 1.1 |
| 3 | W 5/9 | Digital representation of information, Effect of noise on the reliability and choice of digital system. Numbering Systems, Weighted Number Systems, the Radix, Radix Point. | 1.1 & 1.2 |
| 4 | S 8/9 | Binary, Octal and Hexadecimal systems, Important Properties. Number Base Conversion, Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. | 1.2 & 1.3 |
| 5 | M 10/9 | Conversion between binary, Octal and Hexadecimal. Converting Fractions, Binary Addition, Subtraction. | 1.3 |
| 6 | W 12/9 | Binary Multiplication, Hexadecimal Addition and Subtraction, Binary Codes for Decimal Digits, Character Storage, ASCII Code. | 1.3-1.6 |
| 7 | S 15/9 | ASCII Code. Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations. | 2.1, 2.2 |
| 8 | M 17/9 | Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle, Operator Precedence. Properties of Boolean Algebra, Algebraic Manipulation. | 2.1, 2.2 |
| 9 | W 19/9 | Algebraic Manipulation **(Quiz#1)** | 2.1, 2.2 |
| 10 | S 22/9 | Saudi National Day. |  |
| 11 | M 24/9 | MinTerms, MaxTerms, Expressing Functions as a Sum of Minterms, as a Product of Maxterms. Operations on functions performed as operations on minterms. | 2.3 |
| 12 | W 26/9 | Canonical Forms, Standard Forms, Two-Level Implementations of Standard Forms. **(Quiz#2)** | 2.3 |
| 13 | S 29/9 | Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. Propagation Delay, Timing Diagrams.  | 2.9, 3.2 |
| 14 | M 1/10 | Propagation Delay, Timing Diagrams, Fanin Limitations, Fanout Limitations, Use of High- Drive Buffers, Use of Multiple Drivers, Gates with Tri-State Outputs. | 2.10, 6.1, 6.2 |
| 15 | W 3/10 | ***Map method of simplification***: Two-, and Three-variable K-Map. Introduction to Logic Works.  | 2.4 |
|  | Th. 4/10 | **Major Exam I** |  |
| 16 | S 6/10 | ***Map method of simplification***: Three-variable & Four-variable K-Map. Implicants, Prime Implicants, Essential Prime Implicants. | 2.4, 2.5 |
| 17 | M 8/10 | Simplification procedure, POS simplification | 2.5 |
| 18 | W 10/10 | SOP Simplification procedure using Don’t Cares, Five-variable K-map simplification. | 2.5 |
|  | W 10/10Makeup | Six-variable K-map simplification, ypes of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate, universal gates, Two-Level Implementation using Nand/Nor gates. | 2.7 & 2.8 |
|  | W 10/10 | **Last Day for Dropping with W** |  |
| 19 | S 13/10 | Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations. Properties of XOR/XNOR Operations, XOR/XNOR for >2 Variables. The Odd & Even Functions, Parity Generation and Checking. | 2.8 |
| 20 | M 15/10 | Combinational Logic Circuits, Combinational Circuits Design Procedure. BCD to Excess 3 Code Converter. BCD to 7-Segment Decoder for LED. | 3.1-3.3 |
| 21 | W 17/10 |  |  |
|  | 18/10-2/11 | **Eid** **Al-Adha Vacation** |  |
| 22 | S 3/11 | Hierarchical Design, Iterative Arithmetic Combinational Circuits, Iterative equal and magnitude comparator design, Adder Design. Half Adder, Full Adder, 4-bit Ripple Carry Adder. | 5.1-5.2 |
| 23 | M 5/11 | 4-bit RCA: Carry Propagation & Delay, Carry Lookahead Adder, Delay for the 4-bit CLA Adder. | 5.1-5.2 |
| 24 | W 7/11 | Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. Overflow detection. | 5.3 |
| 25 | S 10/11 | Building a device Symbol in Logic Works. **(Quiz#3)** |  |
| 26 | M 12/11 | overflow detection, sign extension, Adder/Subtractor for Signed 2’s Complement. BCD Adder, Binary Multiplier. | 5.3-5.5 |
| 27 | W 14/11 | Enabling Function, Decoders, Hierarchical design of decoders, Implementing Functions using Decoders. Introduction to encoders. | 4.2, 4.3, 4.6 |
| 28 | S 17/11 | **Encoders**: Priority Encoders. **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones.Function implementation using multiplexers. | 3.8, 3.9 |
| 29 | M 19/11 | Demultiplexer. Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Selecting the larger of two 4-bit numbers, Absolute Value of a number. BCD to Excess-3 Code Converter using a decoder and straight binary encoder, Shifter Design, multiplication and division by a constant. | 4.6, 5.6 |
| 30 | W 21/11 | Review for Major Exam II.  |  |
|  | W 21/11 | **Last Day for Dropping all Courses with W** |  |
|  | Th. 22/11 | **Major Exam II** |  |
| 31 | S 24/11 | Introduction to Sequential Circuits, Types of sequential circuits: Synchronous vs. Asynchronous, NOR Set–Reset (SR) Latch. | 6.1-6.2 |
| 32 | M 26/11 | NAND Set–Reset (SR) Latch, Clocked (or controlled) SR NAND Latch, D Latch. Timing Problem of the transparent Latch. | 6.1-6.2 |
| 33 | W 28/11 | Timing Problem of the transparent Latch, Flip flops, S-R Master-Slave (Pulse-Triggered) Flip-Flop, Problems with the S-R Master-Slave Flip-Flop, Edge-Triggered D-type Flip-Flop. Other types of FFs: JK and T flip-flops. | 6.3 |
| 34 | S 1/12 | Other types of FFs: JK and T flip-flops. Characteristic table, Characteristic equation, Excitation table, Designing flip-flops using other flip-flops. Flip-Flop Timing Parameters: Setup and hold times. | 6.4 |
| 35 | M 3/12 | lip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Speed of sequential circuit. Sequential Circuit Analysis: One-Dimensional State Table. | 6.4 |
| 36 | W 5/12 | Sequential Circuit Analysis: One-Dimensional State Table, Two-Dimensional State Table, Sate Diagram, Moore and Mealy Models. Synchronizing sequence. Synchronous & Asynchronous Reset. | 6.4 |
| 37 | S 8/12 | Sequential Circuit Design Procedure, Serial Adder Design. Sequence Detector.  | 6.5 |
| 38 | M 10/12 | Sequential circuit design examples: Sequential Comparator. (**Quiz#4**) | 6.5 |
| 39 | W 12/12 | Sequential circuit design examples: Two’s complement computation (Mealy & Moore), Serial multiplier by a constant (3x), two sequences detector. | 6.5 |
| 40 | S 15/12 | State Minimization. Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers, | 7.1-7.3, 7.6 |
| 41 | M 17/12 | Shift Register Applications. Counters, Ripple Counter. Up-Down Ripple Counter with Enable & Parallel Load. Synchronous Counters: Serial and Parallel Implementations, Up/Down Synchronous Binary Counting with Enable and Parallel Load. | 7.6-7.7 |
| 42 | W 19/12 | Up/Down Synchronous Binary Counting with Enable and Parallel Load. Modulo N counters. | 7.6-7.7 |
|  | W 19/12 | **Dropping all Courses with WP/WF** |  |
| 43 | S 22/12 | Counters as Frequency Dividers, Designing Synchronous Counters using FSMs, Handling Unused States, Counter with Arbitrary Count Sequence. Programmable Implementation Technologies: Overview, Why Programmable Logic? | 7.6-7.7 & 3.6 |
| 44 | M 24/12 | Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM), Types of ROM Devices, Read Only Memory (ROM) Advantages/Limitations. Logic implementation using ROMs. | 3.6 |
| 45 | W 26/12 | Logic implementation using ROMs. Programmable Array Logic (PAL), Programmable Logic Array (PLA), Memory Devices: Introduction. Capacity of a Memory Device, Basic Types of Memory Devices, RAM Memory. | 3.6 & 9.1-9.2 |
|  | S 29/12 (Makeup) | Types of RAM Memory. Review for Final Exam. | 9.1-9.2 |