KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 202 Digital Logic Design

Term 112 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 28/1	Syllabus & Course Introduction. Information Processing and representation. Digital vs. Analog quantities.	1.1
2	M 30/1	Digitization of Analog signals, Digital representation of information, Effect of noise on the reliability and choice of digital system. Numbering Systems, Weighted Number Systems, the Radix.	1.1 & 1.2
3	W 1/2	Radix Point, Binary, Octal and Hexadecimal systems, Important Properties. Number Base Conversion, Converting Whole (Integer) Numbers, Converting from Decimal to Other Bases, Various Methods of Conversion from Decimal to Binary. Conversion between binary, Octal and Hexadecimal.	1.2 & 1.3
4	S 4/2	Converting Fractions, Binary Addition, Subtraction and Multiplication, Hexadecimal Addition and Subtraction, Character Storage, ASCII Code.	1.3-1.6
5	M 6/2	Error Detection, Parity Bit. Elements of Boolean Algebra (Binary Logic), Logic Gates & Logic Operations, Boolean Algebra, Basic Identities of Boolean Algebra, Duality Principle.	2.1, 2.2
6	W 8/2	Duality Principle, Operator Precedence. Properties of Boolean Algebra, Algebraic Manipulation.	2.1, 2.2
7	S 11/2	Algebraic Manipulation. (**Quiz#1**)	2.1, 2.2
8	M 13/2	MinTerms, MaxTerms, Expressing Functions as a Sum of Minterms.	2.3
9	W 15/2	Functions as a Product of Maxterms, Canonical Forms, Standard Forms, Two-Level Implementations of Standard Forms.	2.3
10	S 18/2	Allowed Voltage Levels, Input & Output Voltage Ranges, Noise Margin. (**Quiz#2**)	3.2
11	M 20/2	Propagation Delay, Timing Diagrams, Fanin Limitations, Fanout Limitations.	2.9, 3.2

12	W 22/2	Use of High-Drive Buffers, Use of Multiple Drivers, Gates with Tri-State Outputs. *Map method of simplification*: Two-, and Three-variable K-Map.	2.4
13	S 25/2	*Map method of simplification*: Three-variable & Four-variable K-Map. Implicants, Prime Implicants, Essential Prime Implicants. Simplification procedure.	2.4, 2.5
14	M 27/2	Simplification procedure, Don't Care Conditions, Simplification procedure using Don't Cares.	2.5
15	W 29/2	Review for Major Exam I.	
	Th. 1/3	**Major Exam I**	
16	S 3/3	SOP Simplification procedure using Don't Cares, POS simplification. Solution of Major Exam I.	2.5
17	M 5/3	Five-variable & six-variable K-map simplification. Types of gates: primitive vs. complex gates. Buffer & Tri-state buffer, Nand gate, Nor gate.	2.5 & 2.7
18	W 7/3	Nand gate, Nor gate, universal gates, Two-Level Implementation using Nand/Nor gates. Complex Gates, Exclusive OR (XOR) Gate, Exclusive NOR (XNOR) Gate, XOR Implementations, Properties of XOR/XNOR Operations.	2.7 & 2.8
	W 7/3	**Last Day for Dropping with W**	
19	S 10/3	Properties of XOR/XNOR Operations, XOR/XNOR for >2 Variables. (**Quiz#3**)	2.8
20	M 12/3	The Odd & Even Functions, Parity Generation and Checking. Combinational Logic Circuits, Combinational Circuits Design Procedure. BCD to Excess 3 Code Converter.	3.1-3.3
21	W 14/3	BCD to 7-Segment Decoder for LED, Hierarchical Design, Iterative Arithmetic Combinational Circuits, Adder Design, Half Adder, Full Adder, 4-bit Ripple Carry Adder.	3.3 &5.1-5.2
22	S 17/3	4-bit RCA: Carry Propagation & Delay, Carry Lookahead Adder, Delay for the 4-bit CLA Adder.	5.1-5.2
23	M 19/3	Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. Overflow detection.	5.3
24	W 21/3	2's complement representation, overflow detection, sign extension, Adder/Subtractor for Signed 2's Complement.	5.3-5.4
	24-28/3	**Midterm Vacation**	

25	S 31/3	BCD Adder, Binary Multiplier, Enabling Function, Decoders, Implementing Functions using Decoders.	5.5, 4.2, 4.3, 4.6
26	M 2/4	**Encoders**: Priority Encoders. **Multiplexers:** 2x1, 4x1.	4.4-4.5
27	W 4/4	Constructing large MUXs from smaller ones. Function implementation using multiplexers.	4.6
28	S 7/4	Demultiplexer. (**Quiz#4**)	4.6
29	M 9/4	Design Examples using MSI Functional Blocks: Adding Three 4-bit numbers, Adding two 16-bit numbers using 4-bit adders, Building 4-to-16 Decoders using 2-to-4 Decoders with Enable, Modular Magnitude Comparator, Selecting the larger of two 4-bit numbers, Absolute Value of a number. BCD to Excess-3 Code Converter using a decoder and straight binary encoder. Introduction to Sequential Circuits.	5.6
30	W 11/4	Introduction to Sequential Circuits, Types of sequential circuits: Synchronous vs. Asynchronous, NOR Set–Reset (SR) Latch, NAND Set–Reset (SR) Latch, Clocked (or controlled) SR NAND Latch, D Latch. Timing Problem of the transparent Latch.	6.1-6.2
	W 11/4	**Last Day for Dropping all Courses with W**	
	Th. 12/4	**Major Exam II**	
31	S 14/4	Timing Problem of the transparent Latch, Flip flops, S-R Master-Slave (Pulse-Triggered) Flip-Flop, Problems with the S-R Master-Slave Flip-Flop, Edge-Triggered D-type Flip-Flop.	6.3
32	M 16/4	Flip-Flop Timing Parameters: Setup and hold times, flip-flop propagation delay. Standard Symbols for Storage Elements, Asynchronous vs. Synchronous reset. (Major Exam II Solution)	6.4
33	W 18/4	Other types of FFs: JK and T flip-flops. Characteristic table, Characteristic equation, Excitation table, Designing flip-flops using other flip-flops, Sequential Circuit Analysis.	6.4&6.5
34	S 21/4	Sequential Circuit Analysis: One-Dimensional State Table, Two-Dimensional State Table, Sate Diagram, Moore and Mealy Models. Synchronizing sequence.	6.4
35	M 23/4	Sequential Circuit Design Procedure, Bit Sequence Recognizer, Mealy vs. Moore Design.	6.5
36	W 25/4	(**Quiz#5**)	

37	S 28/4	Sequential circuit design examples: Sequential Comparator, Serial multiplier by a constant (3x), two sequences detector.	6.5
38	M 30/4	Sequential circuit clock speed, Registers, 4-bit Register, with Clear & Selective Parallel Load by clock gating, Avoiding clock gating. Shift Registers, Shift Register Applications.	6.4 & 7.1-7.3, 7.6
39	W 2/5	Determining maximum speed of sequential circuits, Counters, Ripple Counter. Up-Down Ripple Counter with Enable & Parallel Load.	6.4 & 7.6
40	S 5/5	Synchronous Counters: Serial and Parallel Implementations, Up/Down Synchronous Binary Counting with Enable and Parallel Load. Using Counters as Frequency Dividers. Modulo N counters, Designing Synchronous Counters using FSMs, Handling Unused States, Counter with Arbitrary Count Sequence.	7.6-7.7
41	M 7/5	(**Quiz#6**) Programmable Implementation Technologies: Overview, Why Programmable Logic? Hardware Programming Technologies.	3.6
42	W 9/5	Programmable Logic Configurations: ROM, PAL and PLA Configurations, Read Only Memory (ROM). Read Only Memory (ROM) Advantages/Limitations. Logic implementation using ROMs.	3.6
	W 9/5	**Dropping all Courses with WP/WF**	
43	S 12/5	Programmable Array Logic (PAL), Programmable Logic Array (PLA), Memory Devices: Introduction. Capacity of a Memory Device, Basic Types of Memory Devices, RAM Memory, Types of RAM Memory, Read Only Memory (ROM), Types of ROM Devices, ROM-based Designs.	3.6 & 9.1-9.2
44	M 14/5	Review for Final Exam.	
45	W 16/5	Review for Final Exam.	