KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 202 Fundamentals of Computer Engineering
Term 052 Lecture Breakdown

Lec#	Date	Topics	Ref.
	S 10/9		
1	M 13/2	Introduction. Information Processing, and representation. Digital vs Analog quantities. Number systems: Binary system.	1.1 & 1.2
2	W 15/2	Number Systems. Binary, Octal and Hexadecimal #'s, Number base conversion (Dec to Bin, Oct, and Hex, General). Conv (Bin, OCT, Hex).	1.2 & 1.3
3	Th 16/2	Fraction representation, Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement.	5.3 & 5.4
	S 18/2		
4	S 18/2	Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement. R's and (R-1)'s complement. Number System Arithmetic: Addition.	5.3 & 5.4
5	M 20/2	Number System Arithmetic. Binary arithmetic(Addition, Subtraction & Multiplication). Arithmetic in other systems. Signed Binary Addition and Subtraction. R's Complement. Signed Binary Addition and Subtraction. (R-1)'s Complement.	1.3 & 3.10
6	W 22/2	Decimal Codes: BCD, Excess-3, other codes, BCD Arithmetic, Parity Bits.	1.4
	S 25/2		
7	S 25/2	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Principle of duality.	2.1, 2.2
8	M 27/2	Basic identities of Boolean algebra , DeMorgan's law, Algebraic manipulation.	2.2
9	W 1/3	Algebraic manipulation: Absorption, Consensus.	2.2
	S 4/3		
10	S 4/3	Complement of a function, Canonical and Standard forms, Minterms, Sum of products.	2.2, 2.3
11	M 6/3	Canonical and Standard forms, Maxterms, Products of Sums. **(Quiz#2)**	2.3
12	W 8/3	Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.	2.9
	S 11/3		

13	S 11/3	***Map method of simplification***: Two-, and Three-variable K-Map. Implicants , Prime Implicants, Essential Prime Implicants.	2.4, 2.5
14	M 13/3	***Map manipulation:*** Simplification procedure. Four-variable k-map.	2.4, 2.5
15	W 15/3	***Map manipulation:*** Simplification procedure. Four-variable k-map. Multilevel optimization.	2.4 , 2.5, 2.6
	S 18/3		
16	S 18/3	Introduction to Logic Works and K-map minimization tools. **(Quiz#3)**	2.5
17	M 20/3	POS simplification, Don't care conditions and simplification.	2.5
18	W 22/3	Five-variable & six-variable K-map simplification. ***Implementation using Nand and NOR gates:*** 2-level & Multilevel implementation.	2.7
	S 25/3		
19	S 25/3	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.	2.8
	S 25/3	**MAJOR EXAM I**	
20	M 27/3	Combinational Circuit Design Examples: Absolute Value Computation, Equal & Greater than Comparator.	3.1 & 3.3
21	W 29/3	Solution of Major Exam I.	
	S 1/4		
22	M 3/4	Combinational Circuit Design Examples: Less than Comparator, BCD to Seven Segment Display Conversion, 2-bit Adder Design, Modular Adder Design, Ripple Carry Added Design.	3.3 & 5.1 &5.2
23	W 4/4	Ripple Carry Added Design, Design of Subtractor, Analysis of delay of Ripple Carry Added.	5.1-5.4
	S 8/4		
24	S 8/4	Carry Look-ahead adder.	5.2
25	M 10/4	BCD Adder, Binary Multiplier: 2-bit & 4-bit multiplier.	5.6
26	W 12/4	**Decoders** 2x4, 3x8, 4x16. Designing large decoders from smaller decoders. Function implementation using decoders.	4.3 & 4.6
	S 15/4		
27	S 15/4	**Encoders**: Priority Encoders. Applications of decodres and priority encoders. **Multiplexers:** 2x1, 4x1. Constructing large MUXs from smaller ones. Function implementation using multiplexers.	4.4-4.6
28	M 17/4	Function implementation using multiplexers. Demultiplexers. ALU Design.	4.4-4.6

29	W 19/4	Multiplication and division by constants, Sequential Circuits, Concept of memory elements, Nand-Nand SR-Latch.	5.6 & 6.1 & 6.2
	S 22/4		
30	S 22/4	NOR-NOR SR latch, Clocked SR latch, D-latch.	6.2
31	M 24/4	SR-Latch Oscillation problem, Clocked SR Latch, D-Latch, D Flip-Flop.	6.2 & 6.3
32	W 26/4	SR Flip Flo, JK Flip Flop. Edge Triggered vs. Pulse Triggered Flip Flops.	6.3 & 6.6
	S 29/4		
33	S 29/4	T Flip Flop. **(Quiz#6)**	6.6
34	M 1/5	Analysis o Sequential Circuits. State table, State diagram.	6.4
35	W 3/5	Mealy vs. Moore machine. Synchronizing sequence. Designing flip-flops from other flip-flops.	6.4
	S 6/5		
36	S 6/5	Designing flip-flops from other flip-flops. Sequential circuit design: sequence detector.	6.5
	S 6/5	**MAJOR EXAM II**	
37	M 8/5	Sequential circuit design: sequence detector (overlapping & non-overlapping). Serial adder design.	6.5
38	W 10/5	Sequential Circuit Design of 3X circuit. Implementation using D-FFs. Effect of state assignment on implementation.	6.5
	S 13/5		
39	S 13/5	Sequential Circuit design: Mealy vs. Moore design. Design of up counter using JK-FFs and D-FFs.	6.5
40	M 15/5	Setup, Hold, Flip-flop propagation times. Sequential Circuit Timing: Calculation of maximum clock frequency.	6.4
	M 15/5 Makeup Class	Registers, Registers with parallel load, Shift Registers. Shift register with parallel load, Bi-directional shift register. Synchronous Binary Counters: ***Counters with JK-FF, T, and D-FF.*** Up-Down Binary Counter.	7.1 & 7.6
41	W 17/5	Other counters: *Ripple Counter*, Arbitrary Count Sequence.	7.6
	S 20/5		
42	S 20/5	Use of available counters to build counters of different count., BCD Counter. Memory devices: RAMs & ROMs . Combinational Circuit Implementation with ROM.	7.6 & 3.6
42	M 22/5	Programmable Logic Devices: PLAs, PALs, FPGA'a.	3.6
44	W 24/5	***No lecture.***	

	S 27/5		
45	S 27/5	Review.	