King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)

Term 122 (Spring 2013)

Final Exam

Monday May 27, 2013

8:00 a.m. – 10:30 a.m.

Time: 150 minutes, Total Pages: 10

Name: _____ID: _____ Section: _____

Notes:

- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

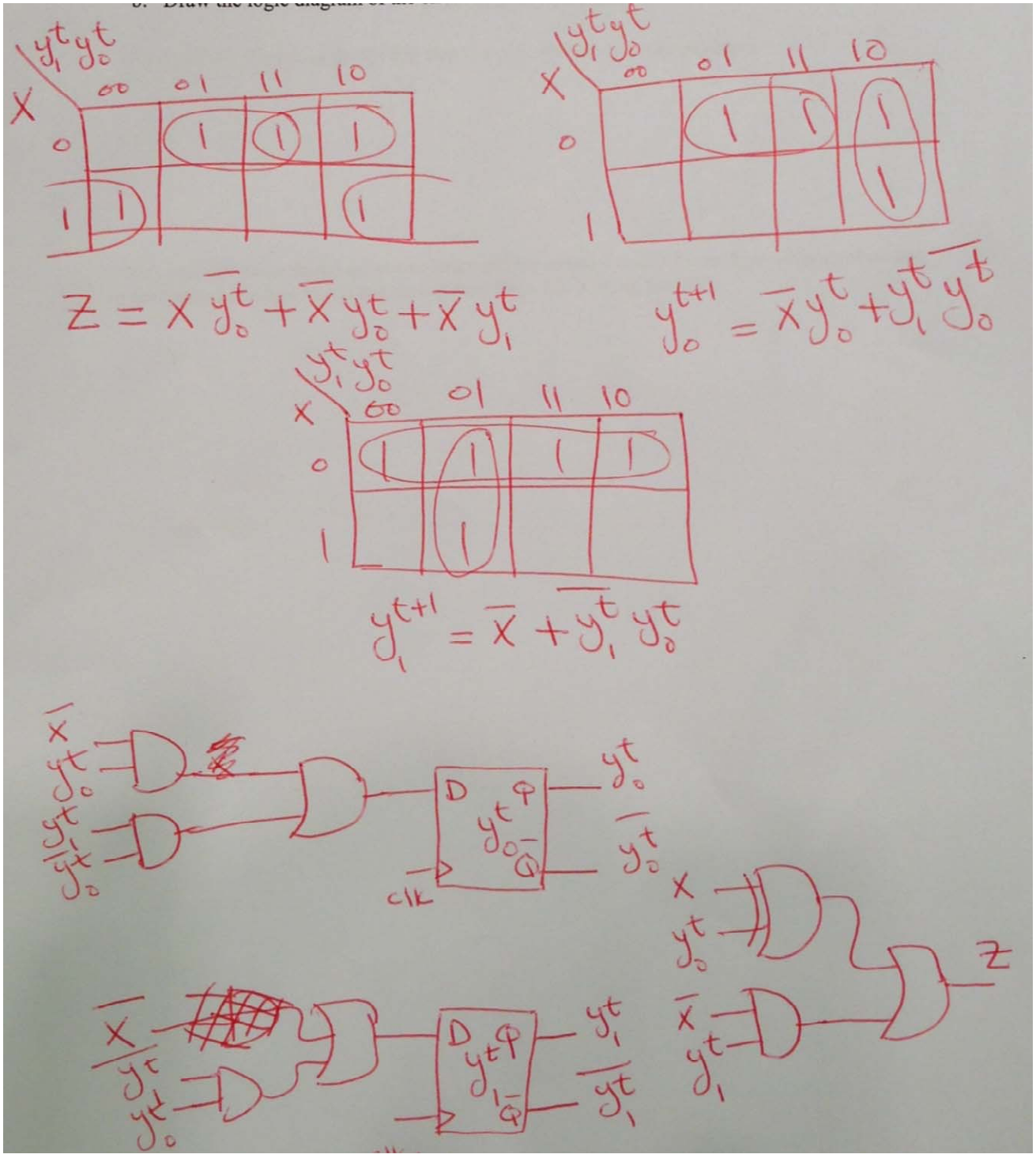
Question	Maximum Points	Your Points
1	10	
2	10	
3	9	
4	9	
5	10	
6	8	
7	14	
8	10	
Total	80	

Question 1. **(10 Points)**

I. A synchronous sequential circuit has a single input x and a single output Z. The state transition table of the circuit is shown.

PS $(y_1\ y_0)^t$	$(y_1\ y_0)^{t+1}$ x = 0	$(y_1\ y_0)^{t+1}$ x = 1	Z x = 0	Z x = 1
0 0	1 0	0 0	0	1
0 1	1 1	1 0	1	0
1 1	1 1	0 0	1	0
1 0	1 1	0 1	1	1

a. Design the circuit using D Flip flops. **(7.5 Points)**
b. Draw the logic diagram of the circuit **(2.5 Points)**

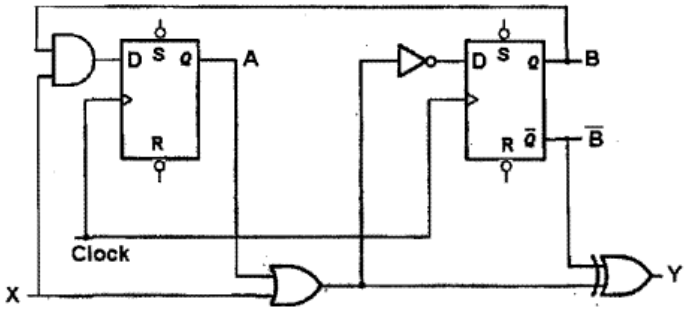


Q2

Consider the sequential circuit shown and answer the following questions:

a. Is the circuit Mealy or Moore?

Mealy



b. Give logical expressions for the D inputs of the flip flop and for the external output

$D_A = X B$

$D_B = \overline{(X + A)} = \bar{X}\,\bar{A}$

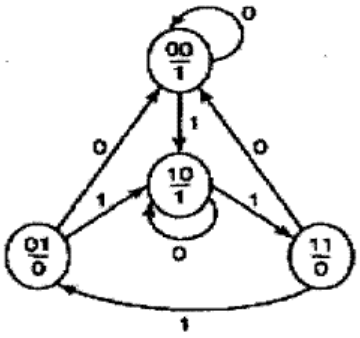
$Y = (X + A) \oplus \bar{B}$

c. Give the state table showing the next state and the external output for each possible combination of ABX (the present state AB and the external input X). X being the LSB.

Present state		I/p	Next state		O/p
A	B	X	A	B	Y
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	1	0	1

Q3

A sequential circuit has the state diagram shown. The circuit has one input X and one output Y. States are given in the format AB where A, B are the state variables.



a. With the circuit in state AB = 11:

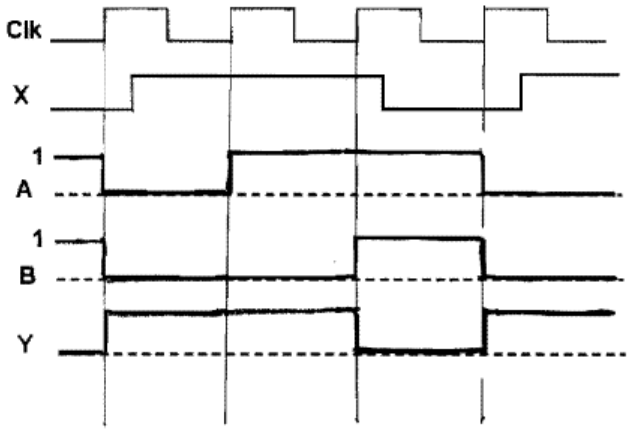
- What is the minimum (non – zero) number of clock pulses required to return the circuit to the same state?

3

- What are the conditions on the input X to achieve this?

X should be kept at 1

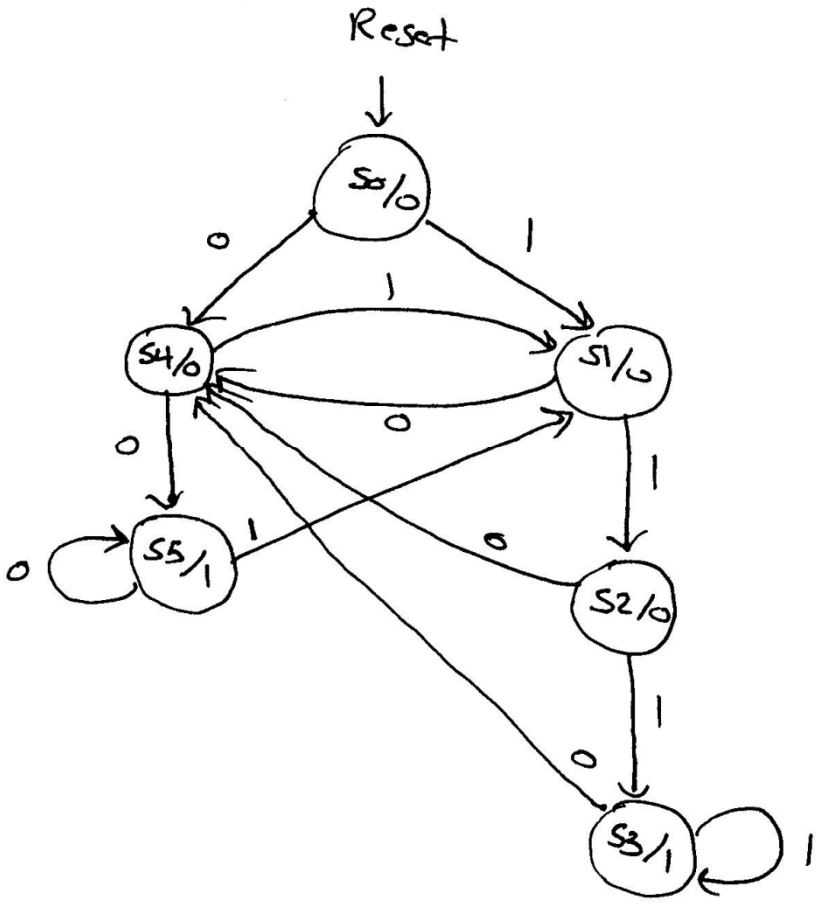
b. Fill in the time traces for A, B, and Y for the given traces for the clock signal and the X input. We start at state AB = 11.



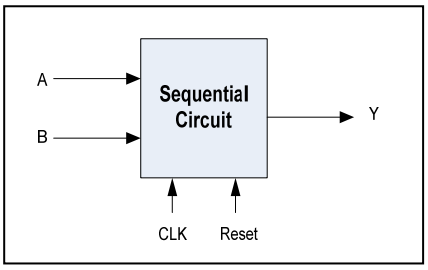
Question 4. **(9 Points)**

It is required to design a synchronous sequential circuit that receives a serial input **X** and produces a serial output **Z**. The output Z will be 1 when the circuit detects **a sequence of <u>three or more consecutive 1's</u> OR <u>two or more consecutive 0's</u>**. Assume the existence of an asynchronous Reset input to reset the machine to a reset state. Draw the <u>state diagram</u> of the circuit assuming a **<u>Moore</u>** model. *You are not required to derive the equations and the circuit.* The following is an example of some input and output data:

Input	**X**	1 1 0 1 1 1 1 0 0 0 1 1 0 0 1 0
Output	**Z**	0 0 0 0 0 0 1 1 0 1 1 0 0 0 1 0



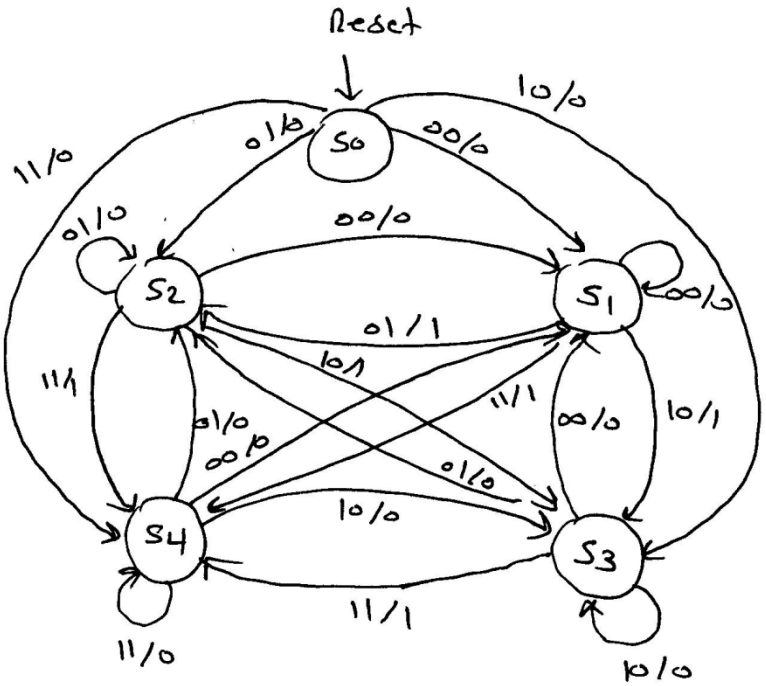
Question 5. **(10 Points)**



It is required to design a sequential circuit that has two inputs A and B, and a single output Y. The circuit receives 2-bit unsigned numbers serially through the inputs A and B. Assume that AB=00=0, AB=01=1, AB=10=2, and AB=11=3. The circuit produces a 1 on the output Y if the current 2-bit number is greater than the previously received 2-bit number. The circuit has an additional asynchronous reset input Reset which resets the circuit into an initial state. Draw the state diagram of the circuit assuming a **Mealy** model. *You are not required to derive the equations and the circuit.*

The following is an example of input and output data:

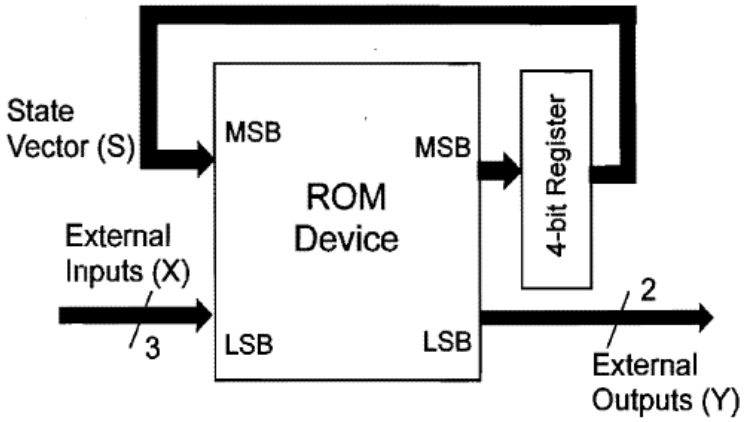
Input	A	0	0	1	0	1	0	0	1	1
	B	1	1	0	1	1	0	1	0	1
Output	Y	0	0	1	0	1	0	1	1	1



Q6

Consider the ROM-Register implementation shown for a Mealy sequential circuit.

Note: Observe the positions indicated on the figure for the LSB/MSB (least/most significant bits) at both input and output of the ROM. The S, X, and Y vectors are always expressed as binary numbers with the LSB being the right-most bit.

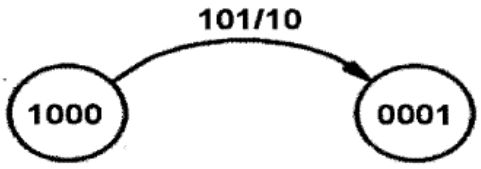


a. The maximum number of states that this sequential circuit can have is $2^4 = 16$.

b. Give that the 4-bit register uses D-type flip flops:

i. The ROM device required should have a minimum of $2^{4+3} = 128$ (how many) storage locations, each being 6 (how many) bits wide.

ii. Refer to the partial state diagram shown for the sequential circuit. With the circuit in state 1000 and inputs X = 101, at the next clock pulse the circuit moves to state 0001 giving outputs Y = 10.



The ROM location being accessed at the above scenario has the binary address 1000101 and the binary contents 000110.

c. If the 4-bit register uses J-K (instead of D-type) flip flops, then:

The ROM device required should have a minimum of 128 (how many) storage locations, each being 8+2=10 (how many) bits wide.

Question 7. **(14 Points)**

Design an up-down mod-16 counter which increments / decrements by 3, e.g. when counting up it counts 0, 3, 6, 9, 12, 15, 2, 5, 8, 11, 14, 1, 4, 7, 10, 13, 0. The counter counts up if an input control signal U equals 1, otherwise it counts down.

The counter should have the following 3 synchronous control inputs:

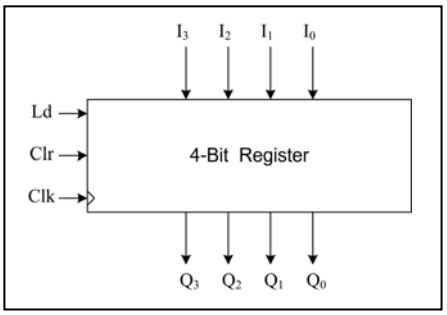
- **i.** CE (Count-Enable) input,
- **ii.** Clr (Clear) input; and
- **iii.** Ld (Load) input which is associated with 4 external inputs (I_3 I_2 I_1 I_0) whose values are parallel-loaded into the counter.

Clr	Ld	CE	U	clk	$(Q_3\ Q_2\ Q_1\ Q_0)^+$
1	X	X	X	↑	0 0 0 0
0	1	X	X	↑	I_3 I_2 I_1 I_0
0	0	0	X	↑	$Q_3\ Q_2\ Q_1\ Q_0$
0	0	1	1	↑	$(Q_3\ Q_2\ Q_1\ Q_0) + 3\ mod\ 16$
0	0	1	0	↑	$(Q_3\ Q_2\ Q_1\ Q_0) - 3\ mod\ 16$

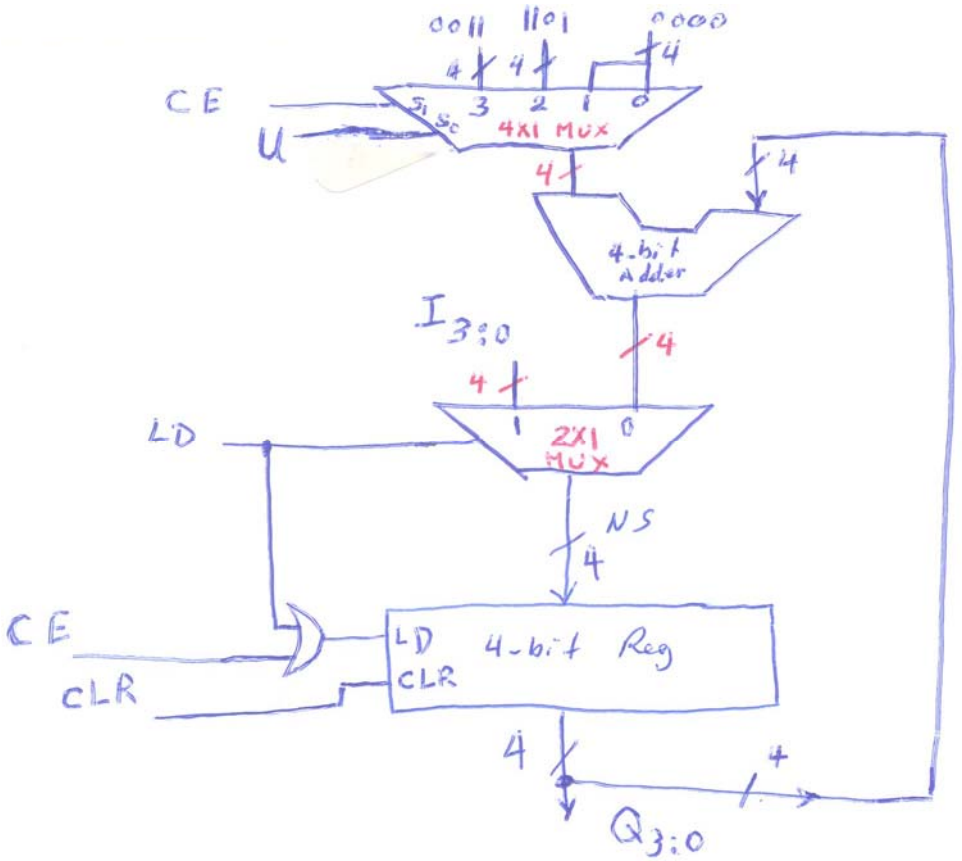
The operation of the counter is described by the function table shown above.

The counter is to be designed using the shown 4-bit register which has synchronous clear (Clr) and synchronous load (Ld) inputs. The function table of this register is given below.

Clr	Ld	clk	$Q_3^+Q_2^+Q_1^+Q_0^+$
1	X	↑	0 0 0 0
0	1	↑	I_3 I_2 I_1 I_0
0	0	↑	$Q_3\ Q_2\ Q_1\ Q_0$

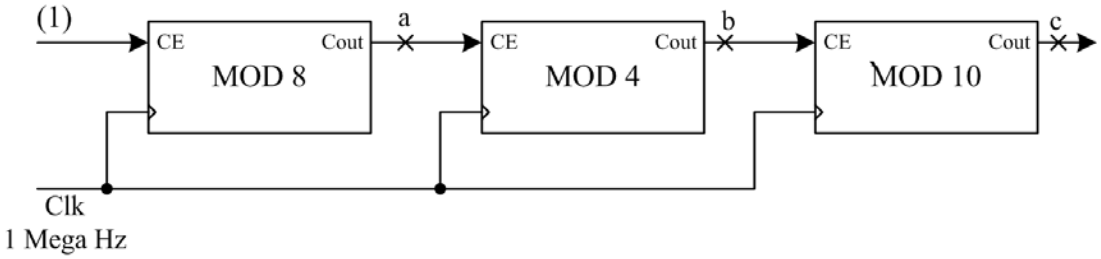


Design the counter **using** this **register** together with a **4-bit binary parallel adder**, a single **OR** gate and **any other MSI parts**.



Question 8. **(10 Points)**

I. For the cascaded counters shown in figure, if the clock frequency is **1 Mega Hertz**, determine the frequency of the signals at nodes **a**, **b** and **c**
(**Note**: CE = Count Enable input, the Cout output is always 0 except when the counter reaches its max count, i.e. 111 for the mod 8, 11 for the mod 4 and 1001 for the mod 10).



$f_{clk} = 1\ MHZ$

$f_a = \frac{f_{clk}}{8} = \frac{1}{8}\ MHz = 125\ KH3$

$f_b = \frac{f_a}{4} = 31.25\ K.Hz.$

$f_c = \frac{f_b}{10} = 3.125\ KHz$

II. For the shown register, assuming an initial state of $(Q_2\ Q_1\ Q_0) = 0\ 0\ 1$, fill in the entries of the shown table for the given sequence of input ***x***. Indicate the register contents following each clock pulse.

.

Clock Pulse #	**Value of *x* just <u>Before</u> the arrival of the next clock pulse**	Q_2	Q_1	Q_0
Initial State	0	0	0	1
1	0	**1**	**0**	**0**
2	1	**1**	**1**	**0**
3	1	**1**	**1**	**1**
4