

*King Fahd University of Petroleum and Minerals*  
*College of Computer Science and Engineering*  
*Computer Engineering Department*

**COE 202: Digital Logic Design (3-0-3)**

**Term 121 (Fall 2013)**

**Final Exam**

**Saturday Jan. 5, 2013**

**7:00 p.m. – 10:00 p.m.**

**Time: 180 minutes, Total Pages: 13**

**Name: KEY ID: \_\_\_\_\_ Section: \_\_\_\_\_**

**Notes:**

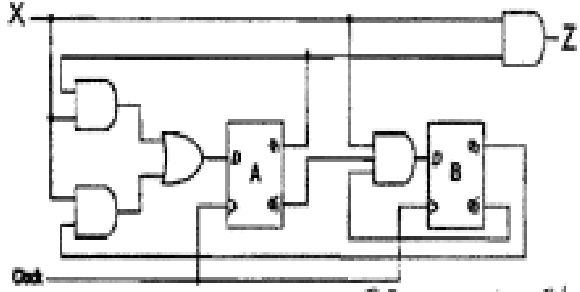
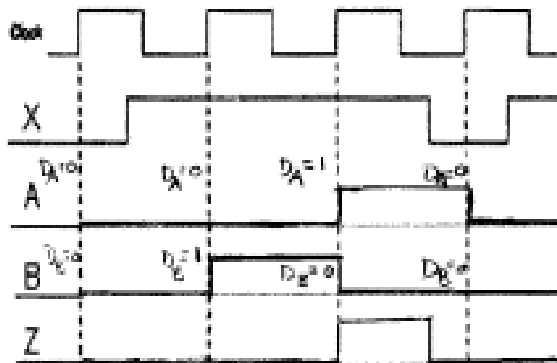
- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

<b>Question</b>	<b>Maximum Points</b>	<b>Your Points</b>
<b>1</b>	<b>20</b>	
<b>2</b>	<b>10</b>	
<b>3</b>	<b>10</b>	
<b>4</b>	<b>12</b>	
<b>5</b>	<b>8</b>	
<b>6</b>	<b>13</b>	
<b>7</b>	<b>7</b>	
<b>8</b>	<b>10</b>	
<b>9</b>	<b>10</b>	
<b>Total</b>	<b>100</b>	

**Question 1.**

**(20 Points)**

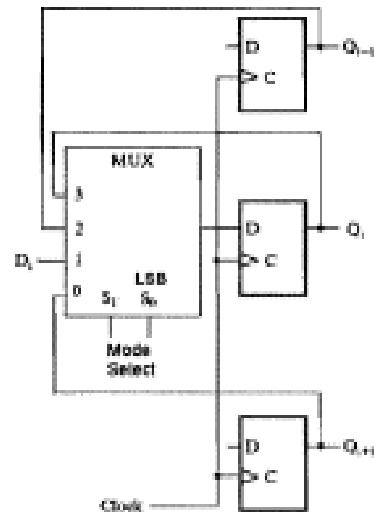
a. The Mealy sequential circuit shown is initially at state  $AB = 00$ . Complete the timing diagram below to show the changes in the state and in the output Z. **(3 Points)**



AB	00	01	10	11
$D_A$	0	0	1	0
$D_B$	0	1	0	0
Z	0	0	1	0

b. The figure opposite shows connection to the flip flop for stage i of a multi-function register. Fill in the spaces in the functional table below: **(5 Points)**

Mode Select I/Ps (S1 S0)	Function
01	Parallel load
11	No Change
00	Shift up
10	Shift down

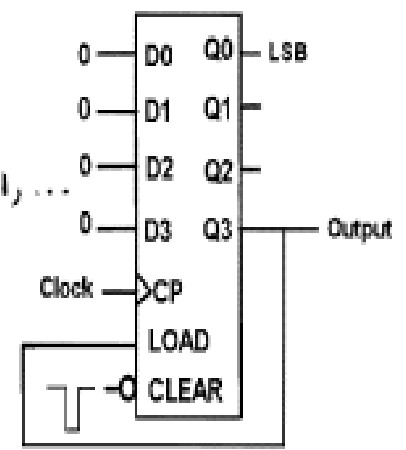


c. Consider the given synchronous counter circuit. The LOAD input is synchronous and the Clear (reset to 0) input is asynchronous. Initially one short 0 pulse is applied at the clear input. **(3 Points)**

*(0, 1, 2, 3, ..., 8, 0, 1, ...)*

- The circuit makes a modulo- 9 counter.
- With a clock input signal having a frequency of 270 pulses/sec, the frequency at the output signal is 30 pulses/sec

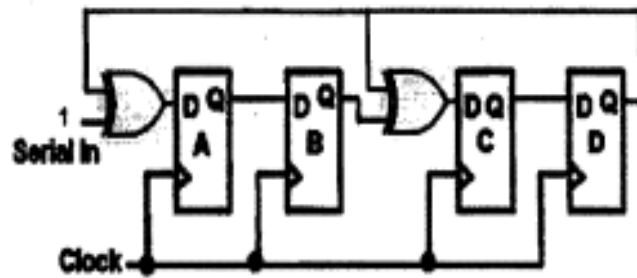
$$\frac{270}{9} = 30$$



d. Consider the 4-bit feedback shift register shown. Initially the register has the contents ABCD = 1101 and the serial input line is kept at 1. After the arrival of two clock pulses, the register contents become ABCD = 1010

(2 Points)

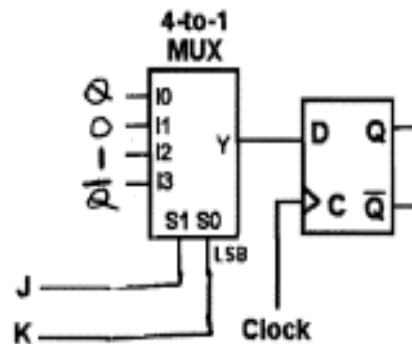
Initial Q | 1101  
 After pulse 1 | 0100  
 " " 2 | 1010



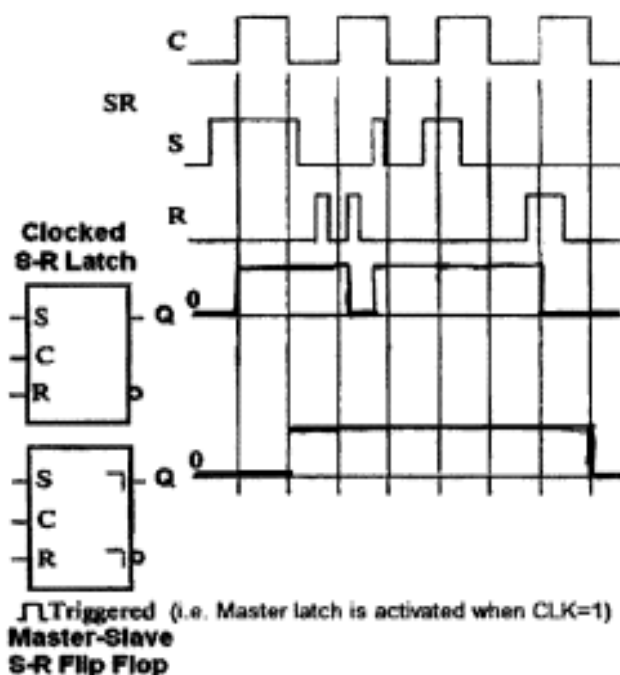
e. The JK flip flop has the characteristic table shown opposite. Complete all connections and show all necessary inputs to the MUX in the figure below to make a JK flip flop using one D-type flip flop and one 4-to-1 multiplexer.

(3 Points)

J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q(t)}$	Complement (Toggle)



f. Sketch the Q outputs for the clocked Set-Reset latch and the Master-Slave Set-Reset flip flop given below for the given input signals. Initially, both Qs are at 0. (4 Points)



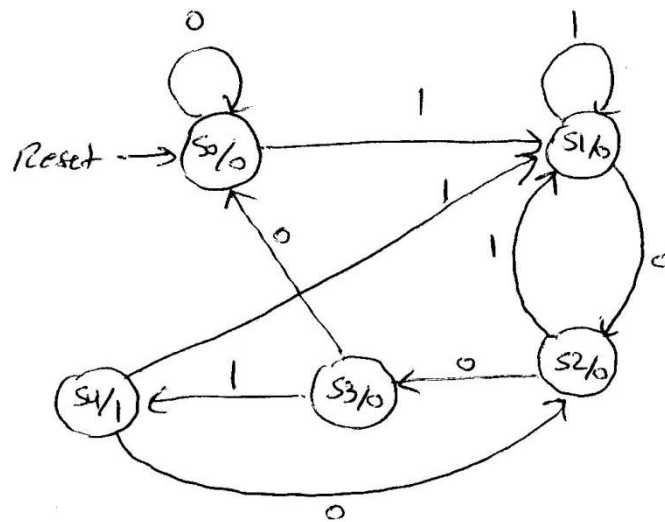
## Question 2.

(10 Points)

It is required to design a sequence detector that detects overlapped occurrences of the sequence **1001**. The circuit receives a serial input **X** and produces a serial output **Z**. The output **Z** will be 1 when the circuit detects the sequence **1001**. Assume the existence of a reset input to reset the machine to a reset state. Draw the state diagram of the circuit assuming a **Moore** model. *You are not required to derive the equations and the circuit.* The following is an example of some input and output streams:

Example:

Input	<b>X</b>	1 0 1 1 0 0 1 0 0 1 1 1 0 0 1 0
Output	<b>Z</b>	0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1



## Question 3.

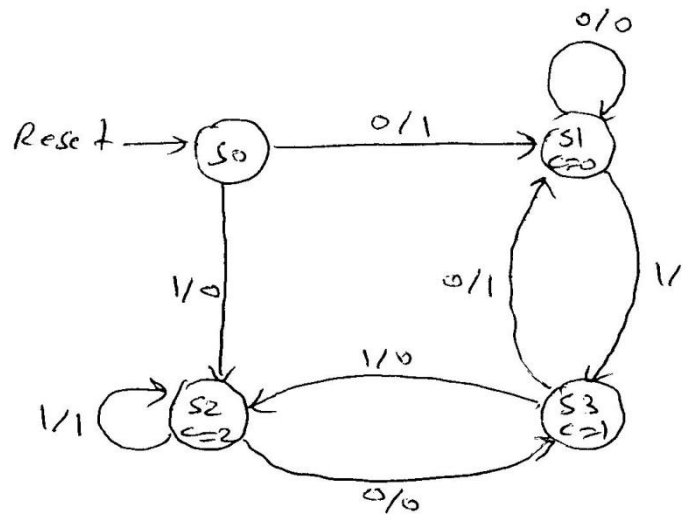
(10 Points)

It is required to design a sequential circuit that has a single input X and a single output Y. The circuit receives an unsigned number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation  $3*X+1$  and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional reset input R which resets the circuit into an initial state. Draw the state diagram of the circuit assuming a **Mealy** model. *You are not required to derive the equations and the circuit.* The following are examples of input and output data:

Examples:

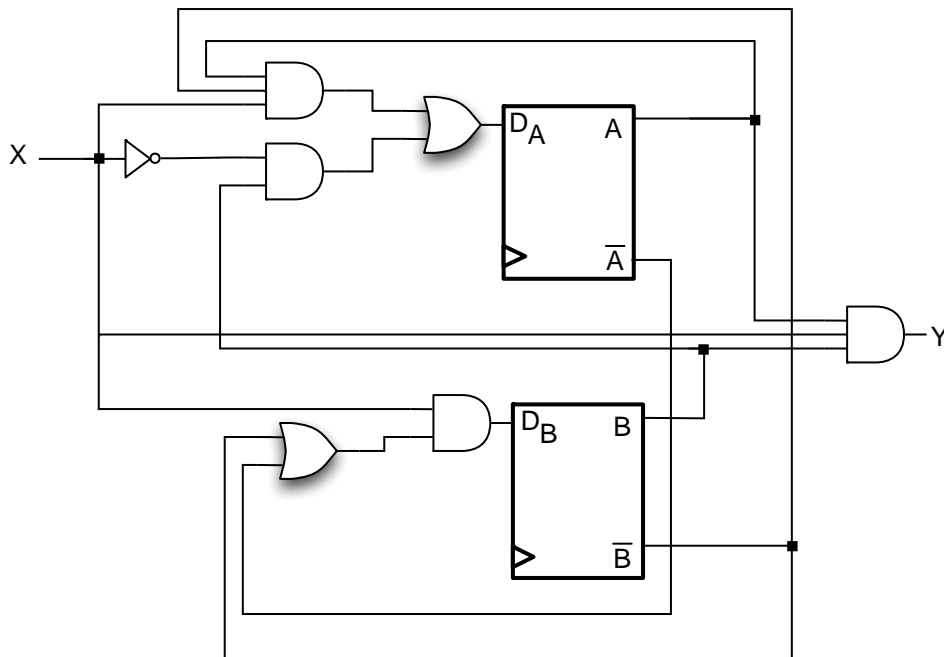
		LSB				MSB		
Input	X	0	1	1	0	0	Input=6	
Output	Y	1	1	0	0	1	Output=19	

		LSB				MSB		
Input	X	1	1	0	0	0	Input=3	
Output	Y	0	1	0	1	0	Output=10	



**Question 4.****(12 Points)**

Consider the sequential circuit below, which has the input X, the output Y and the two D flip-flops A and B.



(a) Is the circuit type Mealy or Moore?

**Mealy**

(b) Derive logic expressions for the  $D_A$  and  $D_B$  inputs of the flip-flops and the external output Y.

$$D_A = XAB' + X'B$$

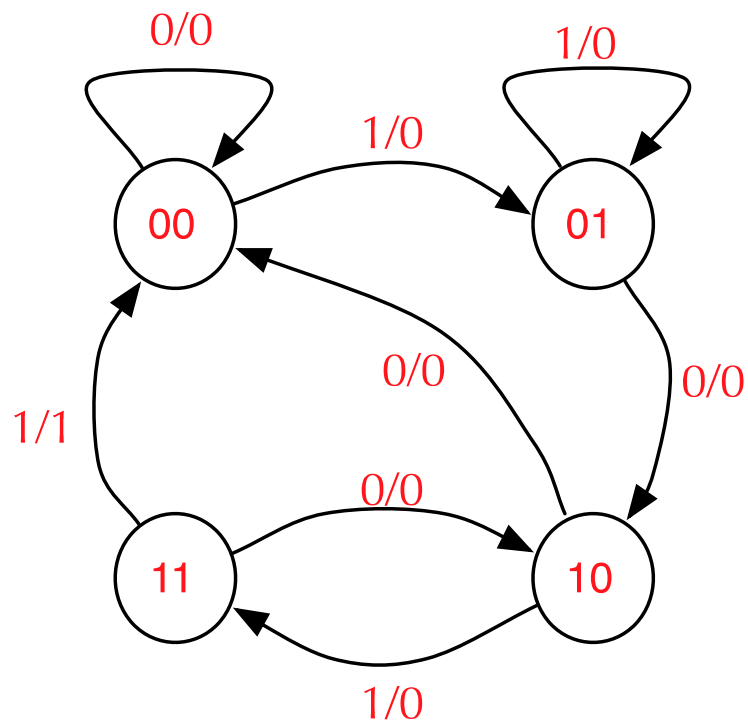
$$D_B = X(A'+B')$$

$$Y = XAB$$

- (c) Provide a state table showing {present state and external inputs} and {next state and external output}.

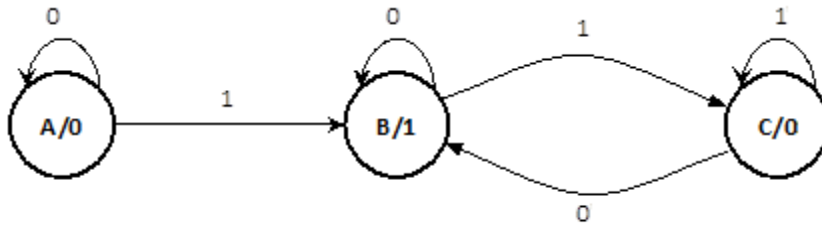
Present State		Input	Next state		Output
A	B	X	A <sup>+</sup>	B <sup>+</sup>	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	0	0	1

- (d) Derive a complete state diagram for the given circuit.



**Question 5.****(8 Points)**

The figure below shows a state diagram of a sequential circuit with one input  $x$  and one output  $y$ . Trace the state transitions of this circuit by determining the output and the next state given the sequence of inputs and an initial state as shown in the tables. Assume that the circuit is reset at state A.



(a)

State	A	A	B	B	B	C	B	C
$x$	0	1	0	0	1	0	1	0
$y$	0	0	1	1	1	0	1	0

(b)

State	A	B	B	C	C	C	B	C
$x$	1	0	1	1	1	0	1	0
$y$	0	1	1	0	0	0	1	0

(c) What is the operation that the above circuit performs on the input  $x$ ? Choose the correct answer:

- i. Multiplication by 2
- ii. Even parity generation
- iii. Odd parity generation
- iv. 2's complement**



**Question 6.****(13 Points)**

The state table of a sequential circuit with 6 states (represented by 000, 001, 010, 011, 100, and, 101), with one Input, X, and two Outputs, Z1 and Z2, is given below. 110 and 111 are not assigned to any state. It is required to implement this circuit using a ROM and D-FFs.

- Choose the don't care outputs to minimize the ROM size and to make sure that if the flip-flops get initialized to 110 or 111, then in subsequent clock pulses the machine will move to one of the valid 6 states.
- Determine the minimal size of the ROM that will be used and show the ROM table. Draw the implementation of this circuit using a ROM and D-FFs. Show all connections and label them accurately.
- If output  $Z_1$  were to be implemented using combinational logic gates, then determine its equation?

Present State			Input	Next State			Outputs	
$Q_A$	$Q_B$	$Q_C$	$X$	$Q_A^+$	$Q_B^+$	$Q_C^+$	$Z_1$	$Z_2$
0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	1	1	1	0
0	1	0	0	0	0	0	0	1
0	1	0	1	1	0	1	0	1
0	1	1	0	1	0	0	1	0
0	1	1	1	0	1	1	0	0
1	0	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0	1
1	0	1	0	0	1	0	0	0
1	0	1	1	0	0	1	1	0
1	1	0	0	0	0	0	0	1
1	1	0	1	0	0	1	0	1
1	1	1	0	0	0	0	0	0
1	1	1	1	0	0	1	0	0

- If don't cares for unused states are properly chosen as shown above then:  
 $Z_2$  can be taken as  $Q_C'$ , and  $Q_C^+$  can be taken as X. All other don't care values are assigned to 0. This ensures that if the flip-flops get initialized to 110 or 111, then in subsequent clock pulses the machine will move to one of the valid 6 states.
- The ROM table for the columns  $Q_A^+$ ,  $Q_B^+$  and  $Z_1$  will be as shown in the table above. Hence, the size of the ROM will be 16 rows and 3 columns.
- $Z_1 = X \cdot Q_A' \cdot Q_B' + X' \cdot Q_A' \cdot Q_C + Q_A \cdot Q_C \cdot X$

**Question 7.****(7 Points)**

It is required to implement the following two functions using a PLA:

$$F_1(A, B, C, D) = \sum m(1, 2, 3, 4, 6, 10, 12, 14) + \sum d(9, 11)$$

$$F_2(A, B, C, D) = \sum m(0, 1, 4, 6, 10, 12, 14) + \sum d(2, 3, 11)$$

Minimize the number of product terms used in the PLA and draw the internal logic of the PLA that will be used to implement these two functions.

$$F_1 = BD' + CD' + B'D$$

$$F_2 = BD' + A'B' + CD'$$

$$F_1' = BD + BC'D'$$

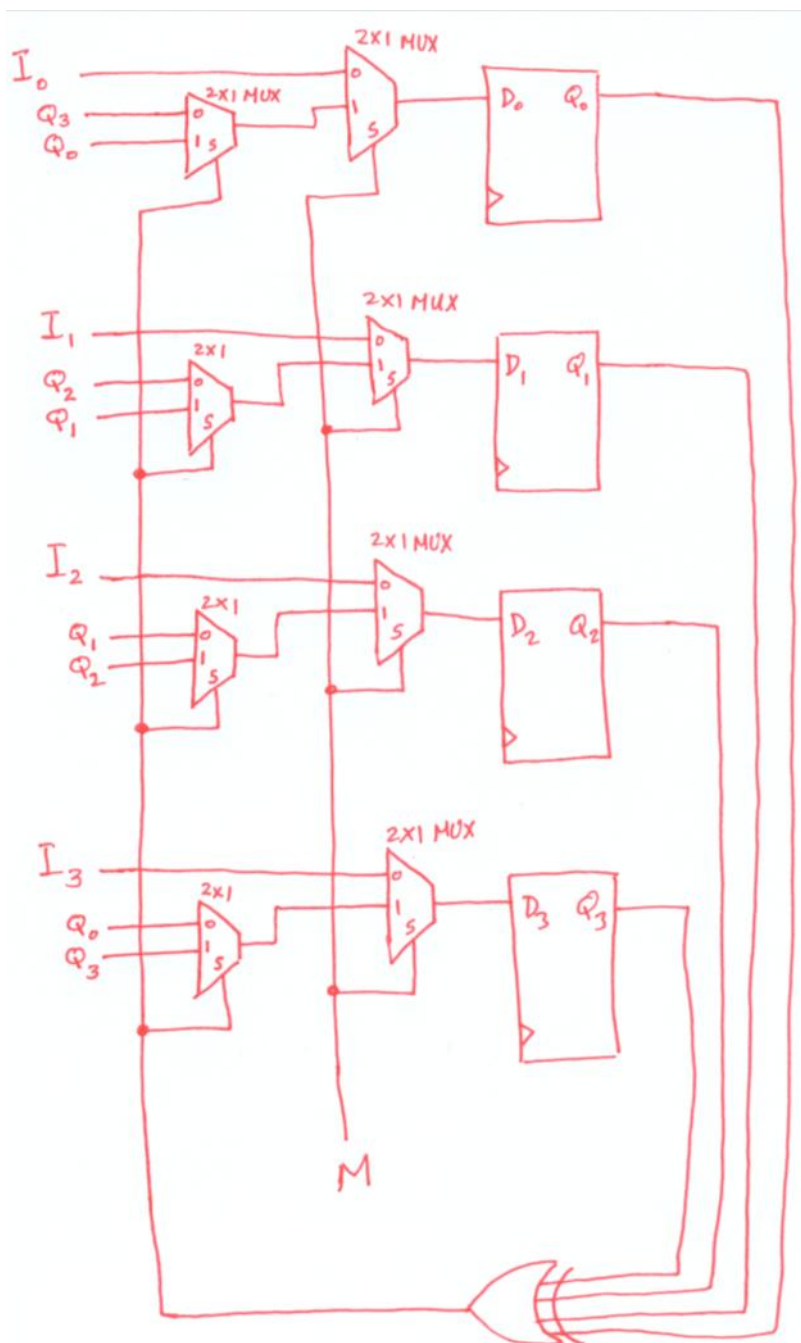
$$F_2' = BD + AB'C'$$

We will use  $F_1'$  and  $F_2'$ , and this will give 3 product terms.  $BD + AB'C' + BC'D'$   
Both outputs are inverted.

**Question 8.****(10 Points)**

Using only D flip-flop(s), MUX(s), and XOR gate(s) draw the logic diagram for a 4-bit register with a mode selection input M. The register should operate according to the following table:

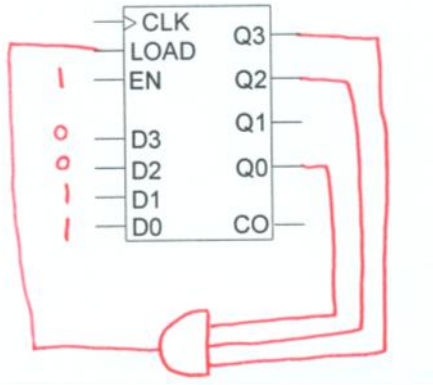
M	Register operation
0	Parallel load
1	Reverse the order of the register bits (i.e., $Q_3^+ = Q_0$ , $Q_2^+ = Q_1$ , $Q_1^+ = Q_2$ , and $Q_0^+ = Q_3$ ) if the current total number of 1s in the register is EVEN. Otherwise, keep the current contents of the register unchanged.



**Question 9.**

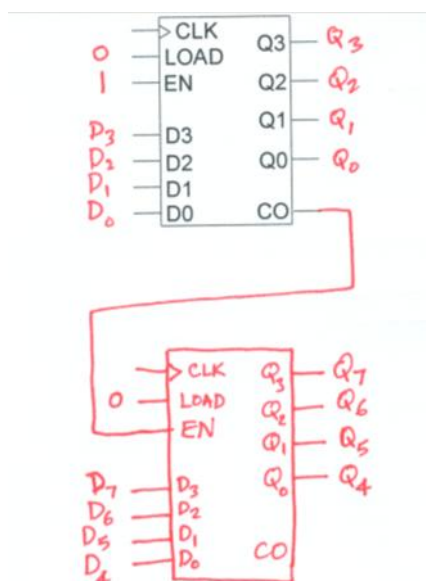
**(10 Points)**

- (a) (3 points) Use minimal external gates and the following counter to design a counter that counts from 3 to 13 and then repeats. Note that the operation of the provided counter is according to the table to the right of the counter. Note also that CO stands for Carry-out which gets set to 1 when the maximum count (i.e. 15) is reached. Assume that the counter is initially loaded with the value 3.



<i>LOAD</i>	<i>EN</i>	<i>Operation</i>
0	0	Hold count
0	1	Increment count
1	X	Parallel load

- (b) (2 points) Use as many of the following counter as necessary to design an 8-bit counter. Properly label Q0 – Q7 and D0 – D7 of the designed counter.



- (c) (5 points) Use minimal external gates and the following 8-bit counter to design a counter that counts from 3 to 29 while skipping the counts from 14 to 18 (that is, count from 3 to 13, then from 19 to 29, and then repeat). Assume that the counter is initially loaded with the value 3.

