

King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)

Term 102 (Spring 2010)

Final Exam

Monday June 6, 2011

7:30 a.m. – 10:00 a.m.

Time: 150 minutes, Total Pages: 14

Name: _____ **ID:** _____ **Section:** _____

Notes:

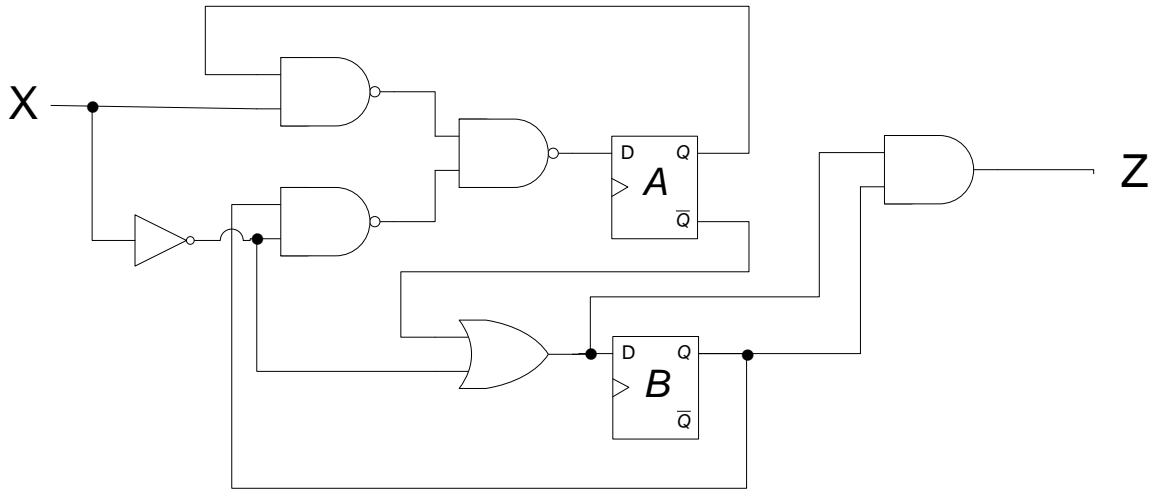
- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	30	
2	25	
3	20	
4	10	
5	20	
Total	105	

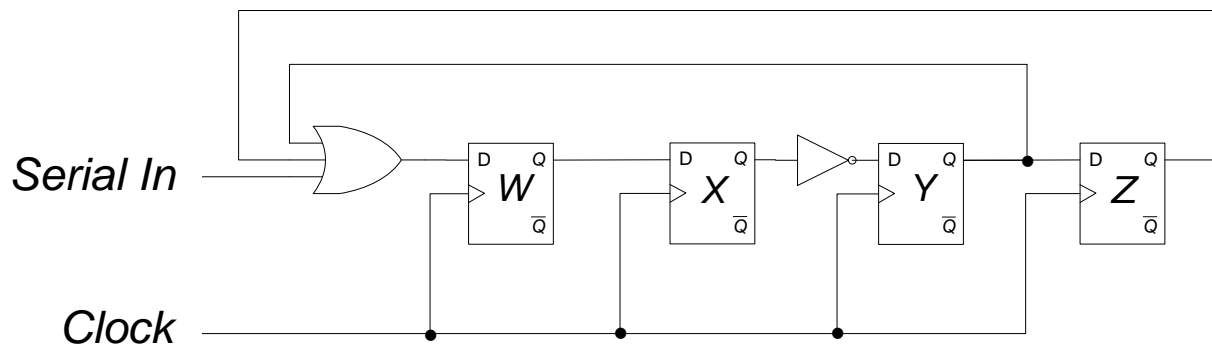
Question 1.

(30 Points)

- a. Derive the state diagram for the following circuit with a single input X , and a single output Z : (10 Points)

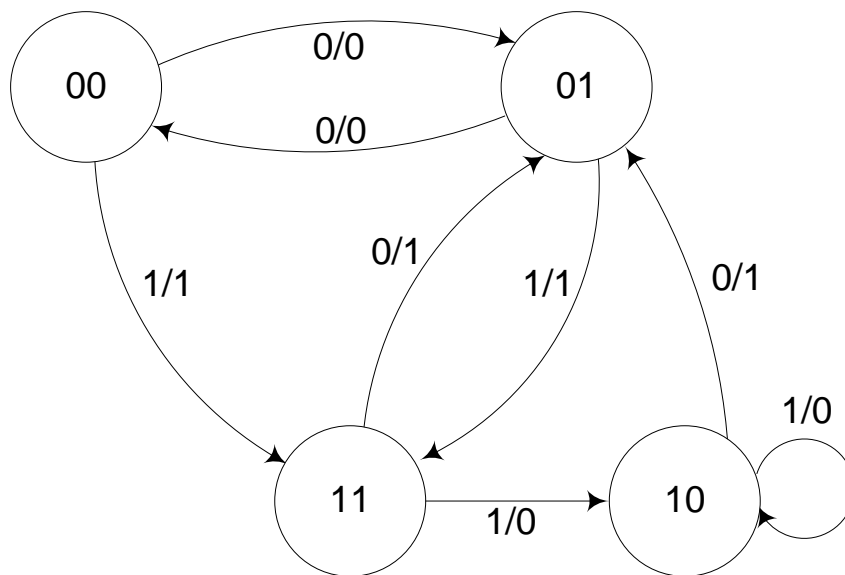
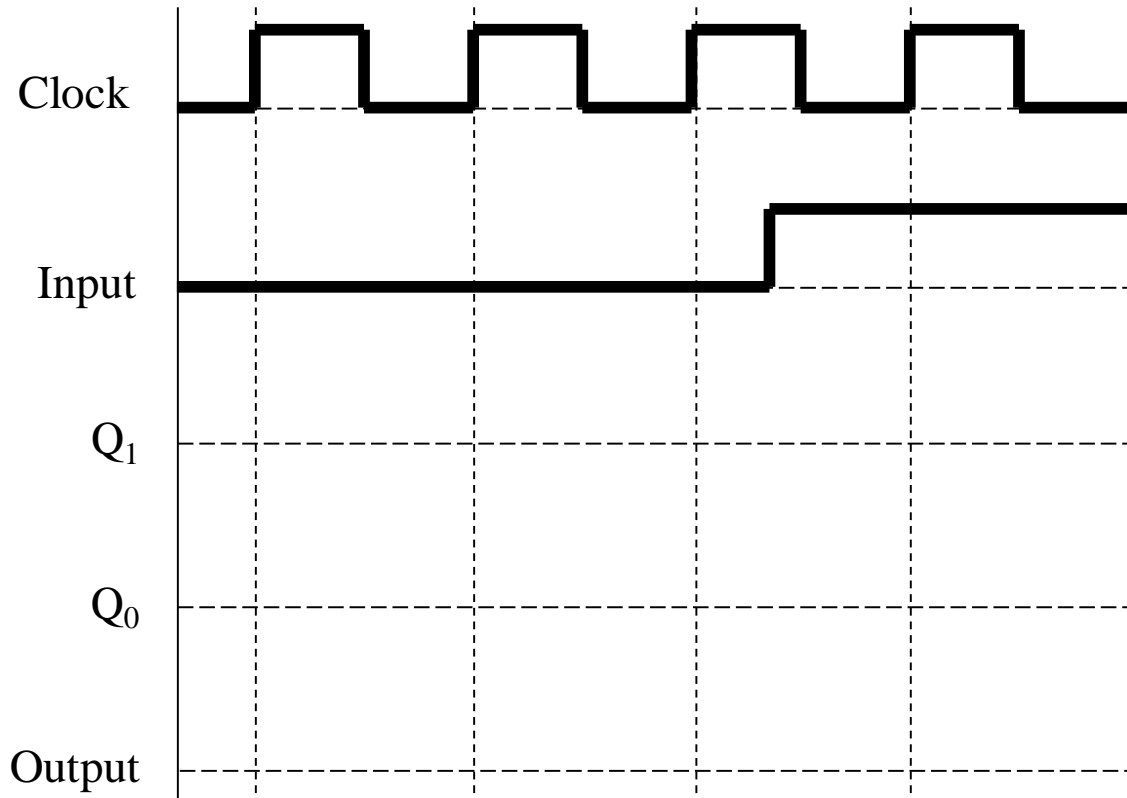


- b. Refer to the shift register circuit shown below where stage Z is the LSB. The circuit has 4 stages of D flip flops and a serial input. Initially the register has the contents WXYZ = 0100. For the sequence of the serial input shown in the table below, fill in the spaces in the table to indicate the register contents following the arrival of each of the next five clock pulses. In the last column, express the contents in HEX. **(8 Points)**



Clock Pulse #	Serial Input, just before the arrival of the next clock pulse	W	X	Y	Z	Register Contents in Hex
Initial State	1	0	1	0	0	4
1	0	1				
2	0					
3	0					
4	0					
5						

c. Complete the following waveform for the positive-edge triggered circuit that implements the state diagram provided below. Assume the circuit is initially at the state $Q_1Q_0 = 00$. **(12 Points)**



Question 2.

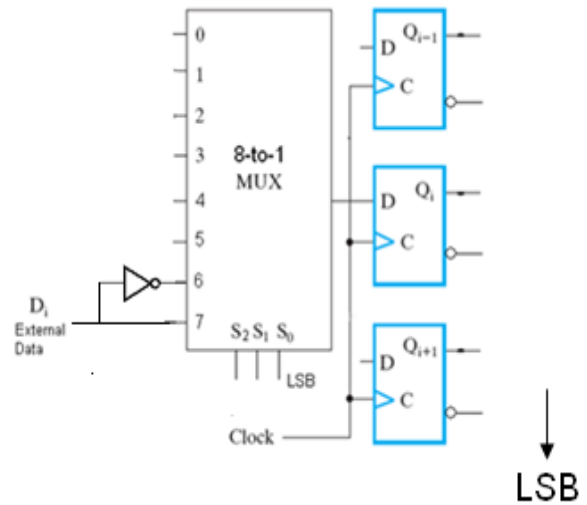
(25 Points)

a. The diagram shows 3 adjacent stages of an n-bit multi-function register that implements 8 functions as shown in the table below. The function is selected by a 3-bit selector S.

- Fill in the two blank rows in the table
- Add to the diagram all missing data/connections.

(8 Points)

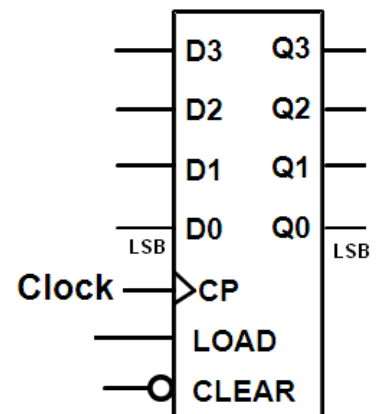
Select Input (S ₂ S ₁ S ₀)	Function Performed
000	Clear register to 0s
001	No change
010	Load register with 2 ⁿ -1
011	Get 1's complement of register contents
100	Shift right (towards LSB)
101	Shift left (towards MSB)
110	
111	



b. Given the 4-bit synchronous binary up counter shown with parallel synchronous input (LOAD) and a direct (asynchronous) CLEAR input:

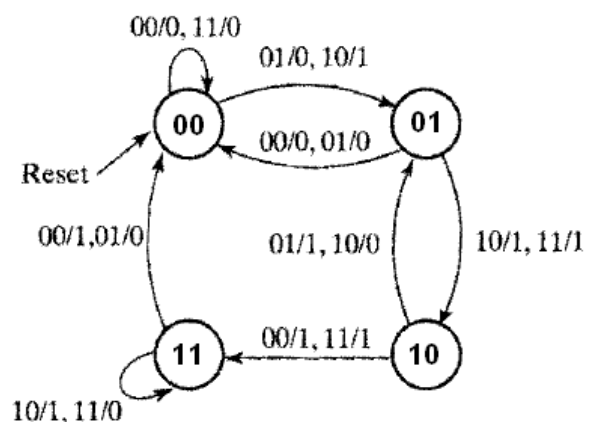
(3 Points)

Add to the figure the logic and connections required to obtain a modulo-12 counter that starts its counting sequence at count 0.

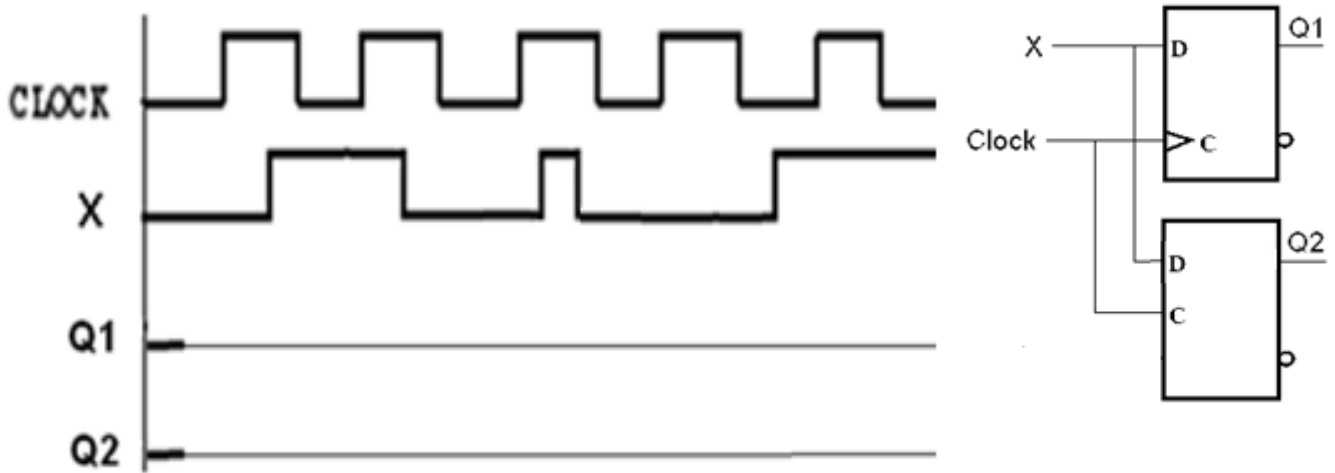


c. A sequential circuit that implements the state diagram shown uses a ROM device for all the combinational logic needed. This ROM should have a minimum of _____ locations, each being _____ bits wide.

(3 Points)



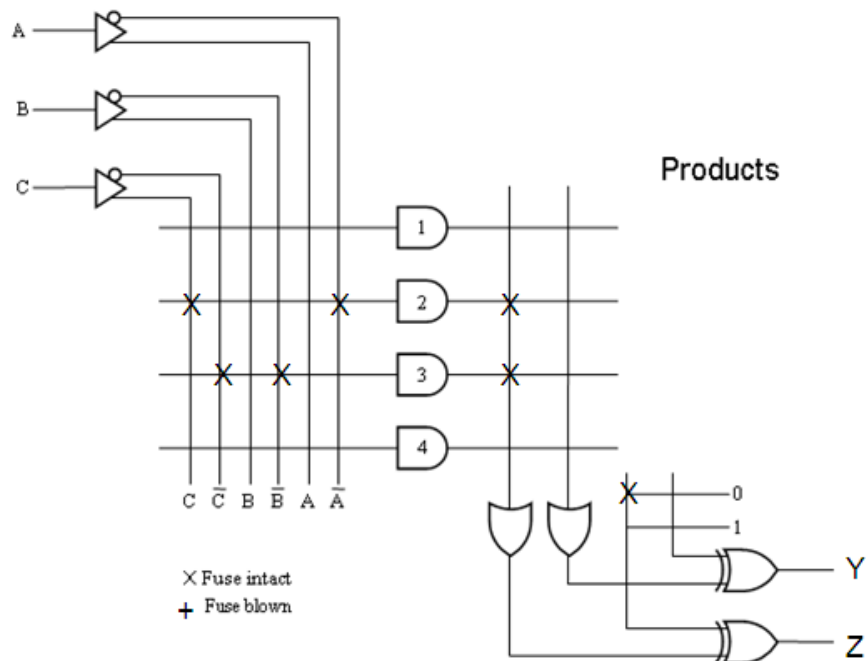
- d. In the circuit shown, the component at the top is a D-type flip flop and the component at the bottom is a clocked D-latch. Plot the waveforms at outputs Q1 and Q2 for the clock and external input waveforms indicated. Assume that both components were initially reset ($Q1 = Q2 = 0$) (5 Points)



- e. Refer to the diagram below for a programmable logic array (PLA) where X indicates a connection.

- Give a logic expression for output Z as a function of the inputs. (3 Points)
- Show all programming connections required to implement output Y as given below: (3 Points)

$$Y = (A + \bar{C})(A + \bar{B} + \bar{C})$$



Question 3.**(20 Points)**

- a. It is required to design a sequence detector that detects overlapped occurrences of the sequence 11011. The circuit receives a serial input **X** and produces a serial output **Z**. The output Z will be 1 when the circuit detects the sequence 11011. Assume the existence of a reset input to reset the machine to a reset state. You are required to derive the state diagram of the circuit assuming **Mealy** model. *You are not required to derive the equations and the circuit.* The following is an example of the input and output streams: **(10 Points)**

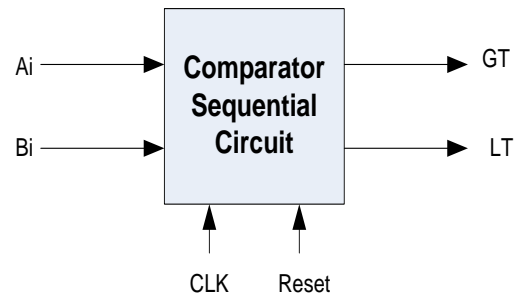
Example

Input	X	0 0 1 1 0 1 1 0 1 1 1 0 1 1 0
Output	Z	0 0 0 0 0 0 1 0 0 1 0 0 0 1 0

- b. It is required to design a sequential circuit that compares two n -bit numbers $A=A_{n-1}A_2A_1A_0$ and $B=B_{n-1}B_2B_1B_0$, applied to the sequential circuit serially from the least significant bits to the most significant bits. The circuit produces two outputs GT and LT. If $A>B$, then the output signal GT is set to 1 and LT is set to 0. If $A<B$, then the output signal LT is set to 1, and GT is set to 0. Otherwise, both signals will be set to 0, which indicates that the two numbers are equal (i.e. $A=B$). Assume the existence of a reset input to reset the machine to a reset state. You are required to derive the state diagram of the circuit assuming **Moore** model. *You are not required to derive the equations and the circuit.* The following is an example of the input and output streams:

(10 Points)

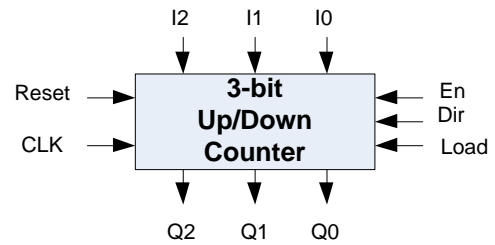
		LSB	MSB
Input	A	0 1 0 0 1 0 1 0	
	B	0 0 0 1 1 0 1 0	
Output	GT	0 0 1 1 0 0 0 0	
	LT	0 0 0 0 1 1 1 1	



Question 4.

(10 Points)

Given the following 3-bit synchronous counter with asynchronous reset signal, **Reset**, to reset it to the all 0 state, an enable signal, **En**, to control whether the counter maintains its state ($En=0$) or enabled to perform desired function ($En=1$), a parallel load signal, **Load**, to load it with any value, a **Dir** signal to control whether the counter counts up or down. When $Dir=0$ the counter counts up otherwise it counts down.



It is required to use this counter to design another counter that works according to the following function table, where **S1** and **S0** are the function select inputs:

S1	S0	Behavior
0	0	No counting
0	1	Parallel Load the counter
1	0	Count Up through the sequence {0, 1, 2, 5, 6, 7}
1	1	Count Down through the sequence {7, 6, 5, 2, 1, 0}

When the counter is counting up and it reaches *count 2, its next count will be 5*. When it is counting down and it reaches *count 5 its next count will be 2*.

Give a block diagram showing all logic or MSI components used, marking clearly all their inputs and outputs.

Question 5.**(20 Points)**

Shown to the right is the state transition table of some synchronous sequential circuit. If the circuit is to be designed using D-FFs, derive

PS ($y_1 \ y_0$) ^t	NS ($y_1 \ y_0$) ⁺		$Z_1 \ Z_0$	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	1 0	0 1	1 1	1 1
0 1	1 0	1 0	1 0	1 0
1 1	1 1	0 0	0 0	0 1
1 0	1 1	0 1	1 1	1 1

- The simplified Boolean expression of all FF inputs. **(4 Points)**
- The simplified Boolean expression of the outputs Z_1 , and Z_0 . **(4 Points)**
- Classify each of the two outputs (Z_1 and Z_0) as either Moore type or Mealy type and **justify**. **(2 Points)**

- d. If the previous circuit is implemented using a single ROM and a single register:

PS ($y_1 \ y_0$) ^t	NS ($y_1 \ y_0$) ⁺		$Z_1 \ Z_0$	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	1 0	0 1	1 1	1 1
0 1	1 0	1 0	1 0	1 0
1 1	1 1	0 0	0 0	0 1
1 0	1 1	0 1	1 1	1 1

- i. Define the size of the required ROM, and its total capacity in bits. **(3 Points)**
- ii. What is the size of the register in bits? **(1 Point)**
- iii. Give the complete ROM Table. **(2 Points)**
- iv. Draw the block diagram of this implementation (**You must CLEARLY LABEL each signal and each component, its inputs and outputs together with all connections**) **(4 Points)**

