*King Fahd University of Petroleum and Minerals*
*College of Computer Science and Engineering*
*Computer Engineering Department*

# COE 202: Digital Logic Design (3-0-3)
## Term 092 (Spring 2010)
## Final Exam
**Sunday June 13, 2010**

**7:30 a.m. – 10:00 a.m.**

**Time: 150 minutes, Total Pages: 11**

**Name: _____ ID: _____ Section: _____**

**Notes:**

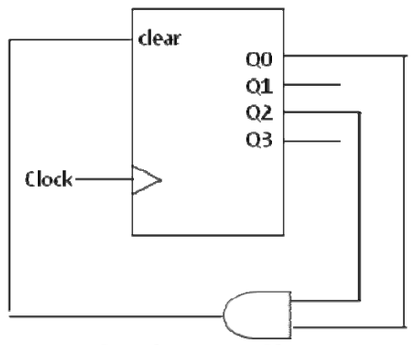
- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

| Question | Maximum Points | Your Points |
|---|---|---|
| 1 | 9 | |
| 2 | 25 | |
| 3 | 15 | |
| 4 | 20 | |
| 5 | 25 | |
| 6 | 6 | |
| Total | 100 | |

**Question 1.** **( 9 points)**

Analyze the following counters and indicate their count ranges in **binary**:

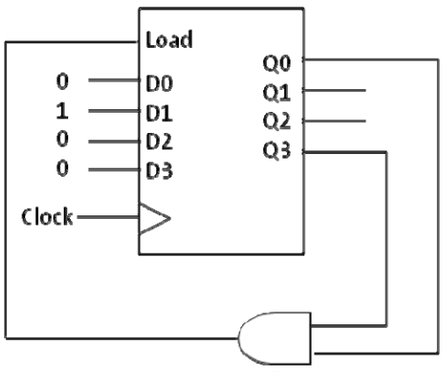
a.




Synchronous Clear

_____ to _____

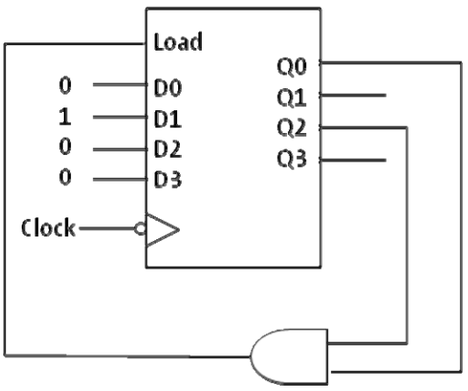
b.




Synchronous Load

_____ to _____

c.



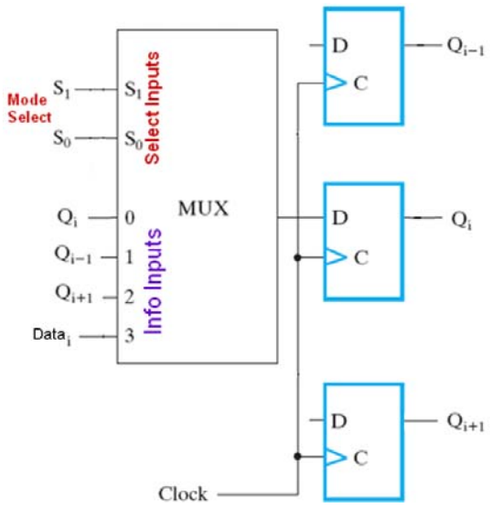

Synchronous Load

_____ to _____

**Question 2.** **(25 Points)**

Fill in the spaces

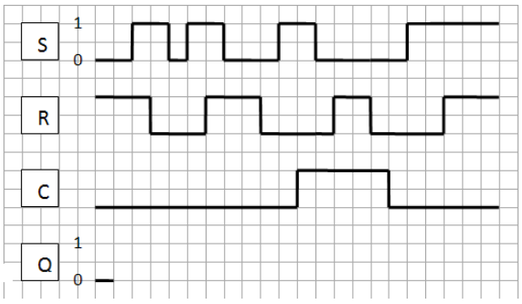
**a**. The figure shows connections to the D input of stage *i* in a multi-function register of D-type flip flops. Study the circuit and then fill in missing information in the table below only for supported register functions.

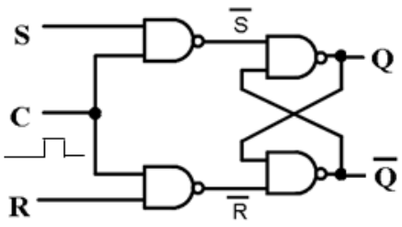



| Mode Select I/Ps (S1 S0) | Register Function (where applicable) |
|---|---|
| | Shift upward |
| | No change in output |
| | Shift downward |
| | Clear register |
| | Load external data input |

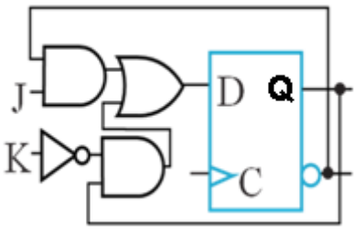
**b**. For the clocked S-R latch using NAND gates shown, complete the waveform of the Q output for the given S, R, and clock (C) inputs.

Initially the Q output is at 0 logic. Ignore any propagation delays.

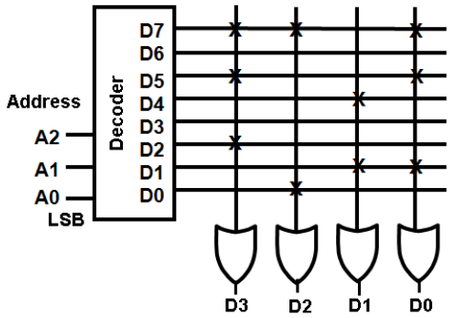



**c**. The flip flop shown is known as the JK flip flop.
For J = 1 and K = 0, the next state of the flip flop Q(t+1) will be Q(t+1) = _____ (select from Q(t), $\overline{Q(t)}$, 0, 1).

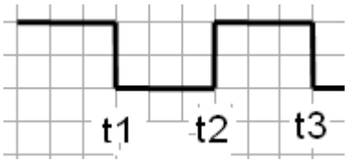


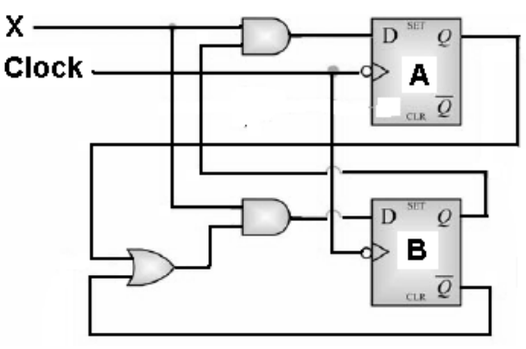

**d**. In the PROM circuit shown, X indicates a connection. At address A2A1A0 = 010, the ROM stores the data D3D2D1D0 = _____.



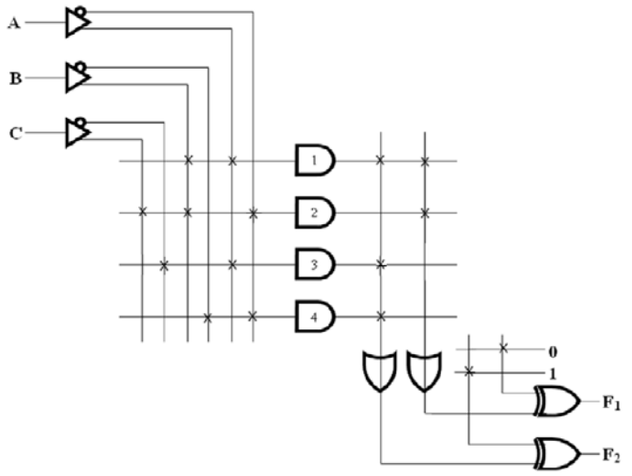

**e**. In the sequential circuit shown, input X = 1. Clock transition **t1** in the figure below puts the circuit in the state AB = 01. Fill in the two spaces in the following table:

| Time | State of the circuit |
|---|---|
| After transition **t2** | |
| After transition **t3** | |



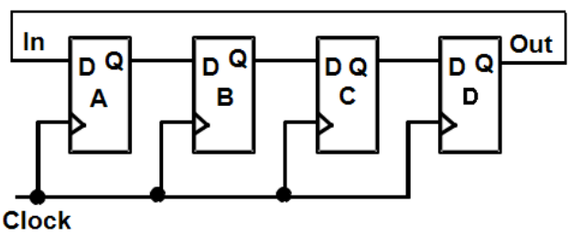
**f**. In the PLA programmable logic device shown, give the algebraic expressions for the logic functions F1 and F2.




F1 =

F2 =

**g**. In the 4-stage shift register shown, the serial output is fed back as the serial input. Initially the register contents (Q outputs) ABCD are 1000. It takes _____ (how many) clock pulses for a '1' to appear at the serial out. At this time, the contents ABCD = _____.




**h**. A memory device has 16 K locations, each being 8-bit wide. This device has _____ (how many) address lines and _____ (how many) data lines.

**Question 3.** **(15 Points)**

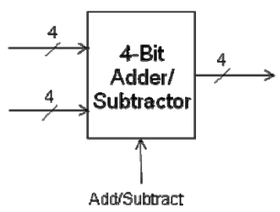
Design a 4-bit up/down binary counter with two control inputs $S_1S_0$. The counter operates according to the shown function table:

| $S_1S_0$ | Function |
|---|---|
| 00 | Stop Counting |
| 01 | Count up |
| 10 | Count down |
| 11 | Initialize the counter to 0 |

You may build the counter with **only** the following three components:

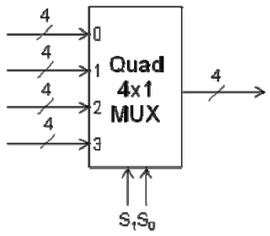
**(1)**

*4-Bit Adder/Subtractor with Add (0)/Subtract(1) control*



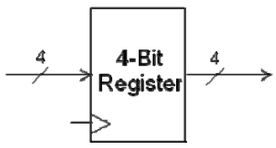

**(2)**

*Quad 4x1 Multiplexer*




**(3)**

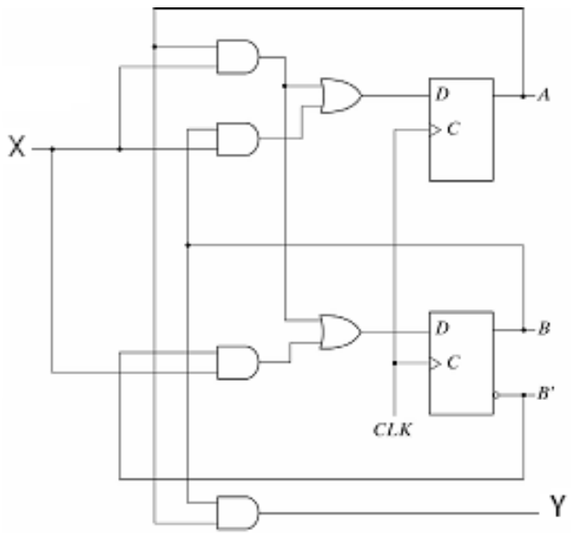
*4-Bit Register*




***Draw a block diagram of your design and clearly label all inputs.***

**Question 4.** **(20 Points)**

Consider the sequential circuit shown and then answer the following questions:



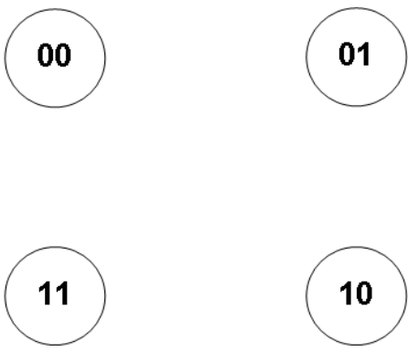

a. Provide Boolean expressions for the D inputs of the flip flops and the external output Y.

b. Is the circuit Mealy or Moore?

c. Use your answer in (a) above to complete the following two-dimensional table state table that gives the next state AB and the external output Y in terms of the present state AB and the external input X.

| Present State AB | Next State AB | | Output Y | |
|---|---|---|---|---|
| | X = 0 | X = 1 | X = 0 | X =1 |
| 00 | | | | |
| 01 | | | | |
| 10 | | | | |
| 11 | | | | |

d. From the state table in c above, complete the state diagram shown below, indicating all state transitions and output values. States are given in the format **AB**.




e. What is the minimum number of clock pulses required to move the circuit from state **AB = 11** to state **AB = 10**?

f. To satisfy the requirement in (e) above, the input X should have the sequence _____.

**Question 5.** **(25 Points)**

A synchronous sequential circuit has a single input x and two outputs $\mathbf{Z_2}$ $\mathbf{Z_1}$. The state transition table of this circuit is given below (same table in 2 different forms).

| Present State y1 y0 | x | Next State | Outputs ( $Z_2$ $Z_1$) |
|---|---|---|---|
| 0 0 | 0 | 0 0 | 1 1 |
| 0 0 | 1 | 0 1 | 1 0 |
| 0 1 | 0 | 1 0 | 0 1 |
| 0 1 | 1 | 1 1 | 0 0 |
| 1 0 | 0 | 0 1 | 1 0 |
| 1 0 | 1 | 1 1 | 1 0 |
| 1 1 | 0 | 0 1 | 0 0 |
| 1 1 | 1 | 1 1 | 0 0 |

| Present State y1 y0 | Next State x = 0 | Next State x = 1 | Outputs ( $Z_2$ $Z_1$) x = 0 | Outputs ( $Z_2$ $Z_1$) x = 1 |
|---|---|---|---|---|
| 0 0 | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 1 | 1 0 | 1 1 | 0 1 | 0 0 |
| 1 1 | 0 1 | 1 1 | 0 0 | 0 0 |
| 1 0 | 0 1 | 1 1 | 1 0 | 1 0 |

a. Provide a minimized design for this circuit using gates and D Flip-Flops,
b. Draw the logic diagram of the circuit.
c. Classify each of the two outputs ($\mathbf{Z_2}$ $\mathbf{Z_1}$) either as Moore type or Mealy type.
d. **If** this synchronous sequential circuit is implemented using a single ROM and a single register:
   i. Define the size of the required ROM, and its total capacity in bits.
   ii. What is the size of the register in bits?
   iii. Define the ROM Truth Table.
   iv. Draw the block diagram of this implementation (**CLEARLY LABEL each element, its inputs and outputs and show how they are connected**)

| **Present State y1 y0** | **x** | **Next State** | **Outputs ( $Z_2$ $Z_1$)** |
|---|---|---|---|
| 0 0 | 0 | 0 0 | 1 1 |
| 0 0 | 1 | 0 1 | 1 0 |
| 0 1 | 0 | 1 0 | 0 1 |
| 0 1 | 1 | 1 1 | 0 0 |
| 1 0 | 0 | 0 1 | 1 0 |
| 1 0 | 1 | 1 1 | 1 0 |
| 1 1 | 0 | 0 1 | 0 0 |
| 1 1 | 1 | 1 1 | 0 0 |

| **Present State y1 y0** | **Next State** | | **Outputs ( $Z_2$ $Z_1$)** | |
|---|---|---|---|---|
| | **x = 0** | **x = 1** | **x = 0** | **x = 1** |
| 0 0 | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 1 | 1 0 | 1 1 | 0 1 | 0 0 |
| 1 1 | 0 1 | 1 1 | 0 0 | 0 0 |
| 1 0 | 0 1 | 1 1 | 1 0 | 1 0 |

d. **If** the previous synchronous sequential circuit is implemented using a ***single*** **ROM** and a ***single*** **register**:
   i. Define the size of the required ROM, and its total capacity in bits.
   ii. What is the size of the register in bits?
   iii. Define the ROM Truth Table.
   iv. Draw the block diagram of this implementation (**CLEARLY LABEL each element, its inputs and outputs and show how they are connected**)

**Question 6.** **(6 Points)**

A sequential circuit has 2 inputs *x* and *y* and an output *Z*. The output equals "1" when it receives 4th occurrence of equal inputs $x = y$ (**not necessarily consecutive**). After receiving these occurrences, the circuit starts counting these occurrences over again. The circuit has an additional reset input R which resets the circuit into the initial state.

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *x* = | 0 | 0 | **1** | 0 | 1 | 1 | **0** | **1** | 0 | **0** | **0** | 1 | **1** | 0 | **0** | 1 | 1 | **1** | 0 |
| *y* = | 1 | 1 | **1** | 1 | 0 | 0 | **0** | **1** | 1 | **0** | **0** | 0 | **1** | 1 | **0** | 0 | 0 | **1** | 1 |
| *Z* = | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 |

**Draw the Mealy state diagram of the circuit**