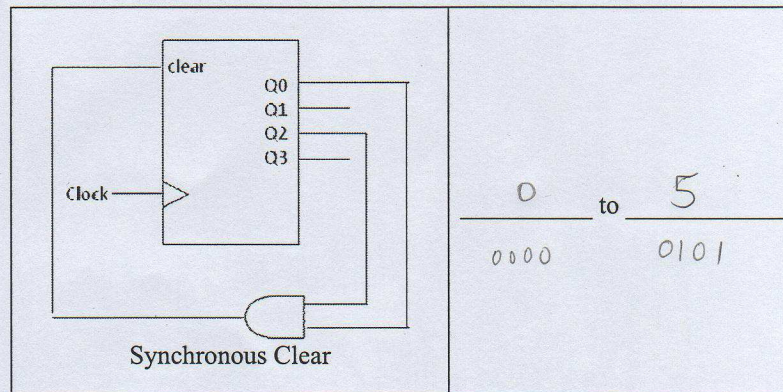
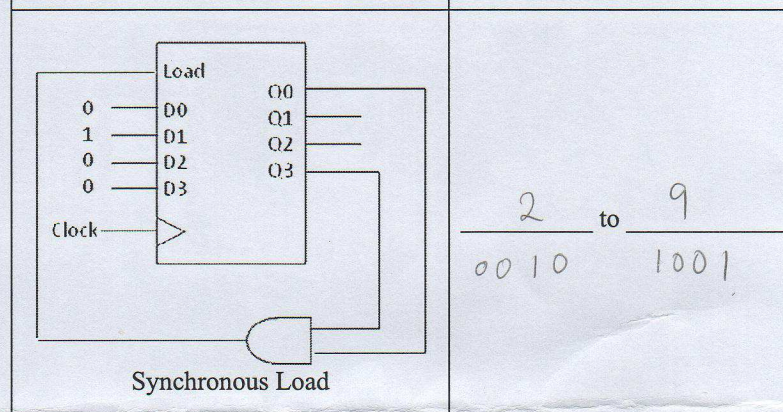


Question 1.**(9 points)**Analyze the following counters and indicate their count ranges in **binary**:

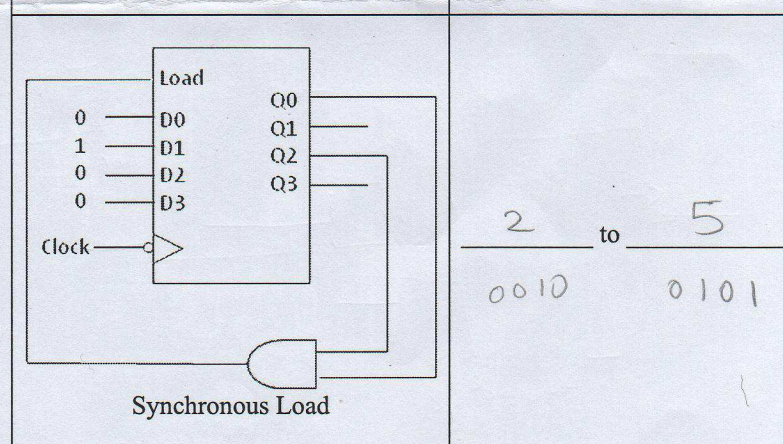
a.



b.



c.



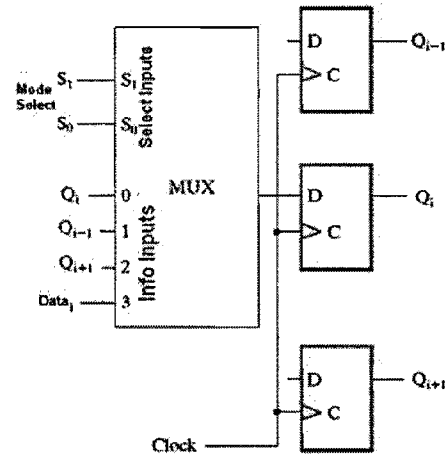
~~Page 2 of 11~~
page 2 of 11

Question 2.

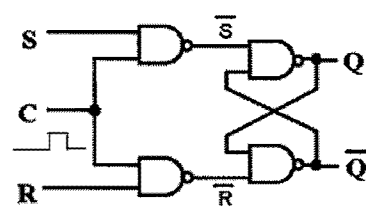
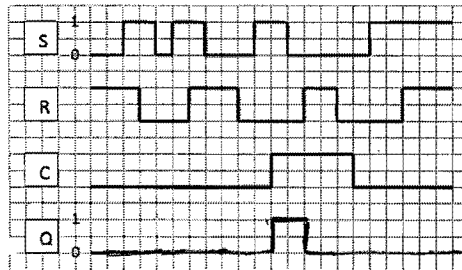
Fill in the spaces

- a. The figure shows connections to the D input of stage i in a multi-function register of D-type flip flops. Study the circuit and then fill in missing information in the table below only for supported register functions.

Mode Select I/Ps (S_1 S_0)	Register Function (where applicable)
1 0	Shift upward
0 0	No change in output
0 1	Shift downward
	Clear register
1 1	Load external data input

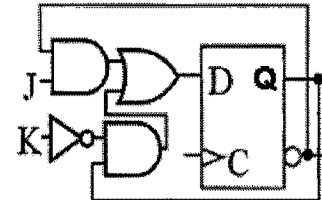


- b. For the clocked S-R latch using NAND gates shown, complete the waveform of the Q output for the given S, R, and clock (C) inputs.

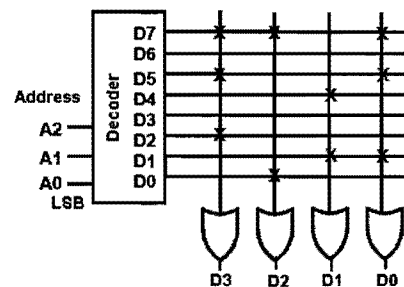


Initially the Q output is at 0 logic. Ignore any propagation delays.

- c. The flip flop shown is known as the JK flip flop.
For $J = 1$ and $K = 0$, the next state of the flip flop $Q(t+1)$ will be
 $Q(t+1) = \underline{\quad 1 \quad}$ (select from $Q(t)$, $\overline{Q(t)}$, 0, 1).

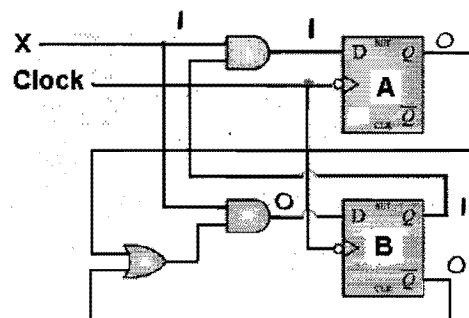
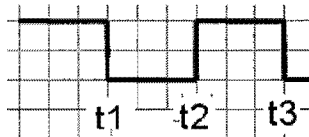


- d. In the PROM circuit shown, X indicates a connection.
At address $A_2A_1A_0 = 010$, the ROM stores the data $D_3D_2D_1D_0 = \underline{1000}$.



- e. In the sequential circuit shown, input $X = 1$. Clock transition t_1 in the figure below puts the circuit in the state $AB = 01$. Fill in the two spaces in the following table:

Time	State of the circuit
After transition t_2	0 1
After transition t_3	1 0

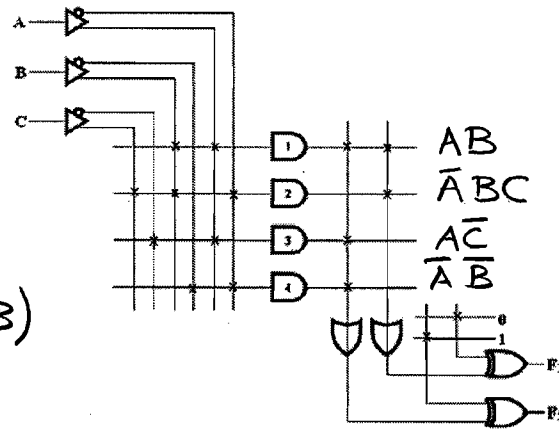


f. In the PLA programmable logic device shown, give the algebraic expressions for the logic functions F1 and F2.

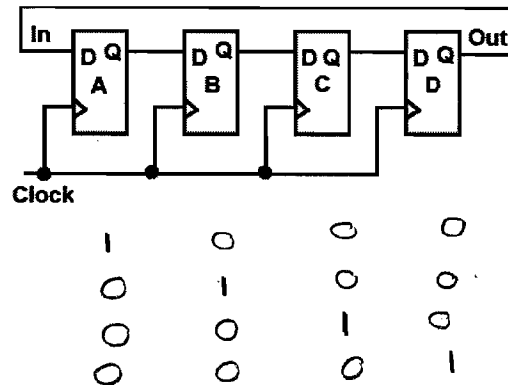
$$F1 = AB + \bar{A}BC$$

$$F2 = AB + A\bar{C} + \bar{A}\bar{B}$$

$$= (\bar{A} + \bar{B}) \cdot (\bar{A} + C) \cdot (A + B)$$



g. In the 4-stage shift register shown, the serial output is fed back as the serial input. Initially the register contents (Q outputs) ABCD are 1000. It takes 3 (how many) clock pulses for a '1' to appear at the serial out. At this time, the contents ABCD = 0001.



h. A memory device has 16 K locations, each being 8-bit wide. This device has 14 (how many) address lines and 8 (how many) data lines.

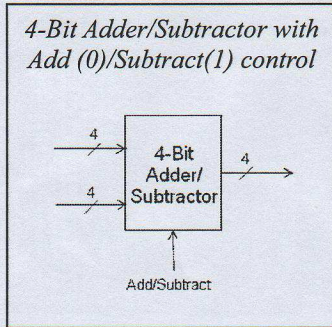
Question 3.

Design a 4-bit up/down binary counter with two control inputs S_1S_0 . The counter operates according to the shown function table:

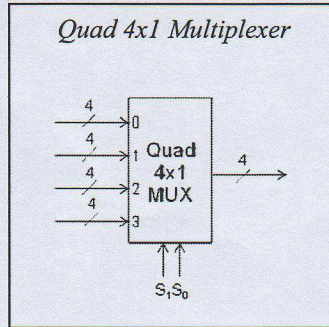
S_1S_0	Function
00	Stop Counting
01	Count up
10	Count down
11	Initialize the counter to 0

You may build the counter with only the following three components:

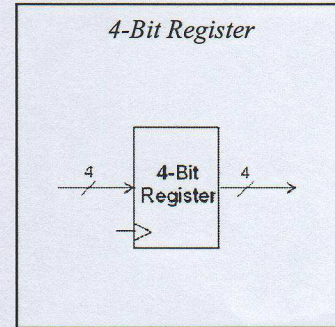
(1)



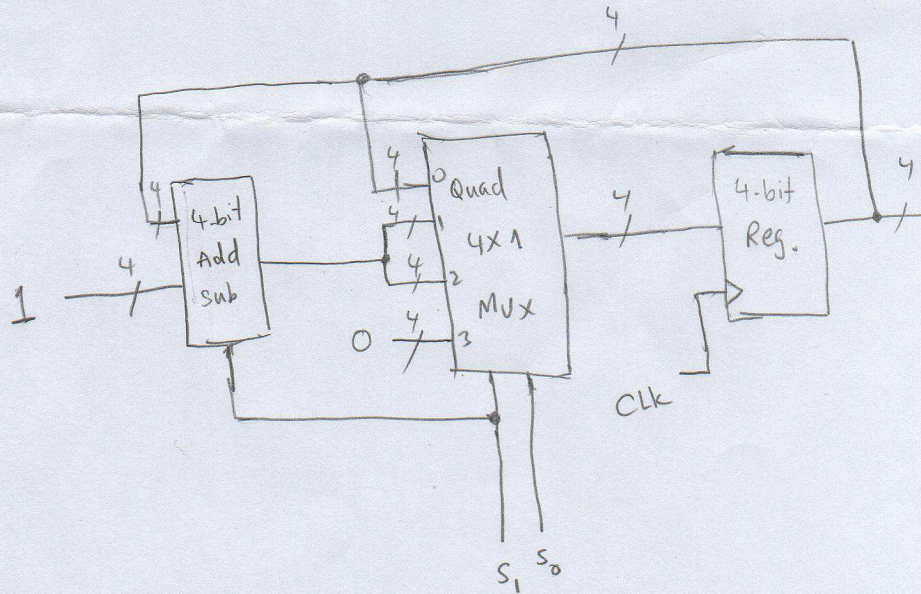
(2)



(3)



Draw a block diagram of your design and clearly label all inputs.



Question 4.

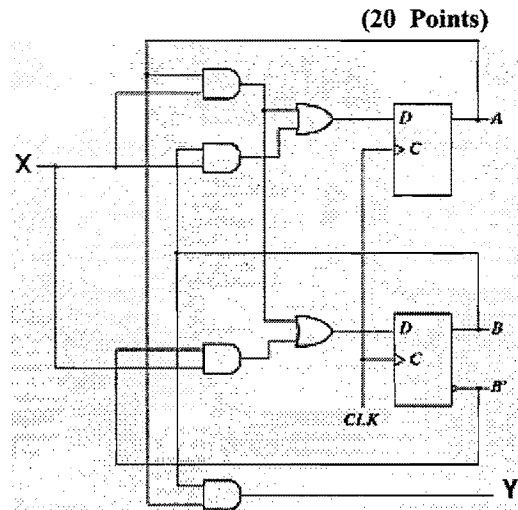
Consider the sequential circuit shown and then answer the following questions:

- a. Provide Boolean expressions for the D inputs of the flip flops and the external output Y.

$$D_A = AX + BX$$

$$D_B = AX + \bar{B}X$$

$$Y = AB$$



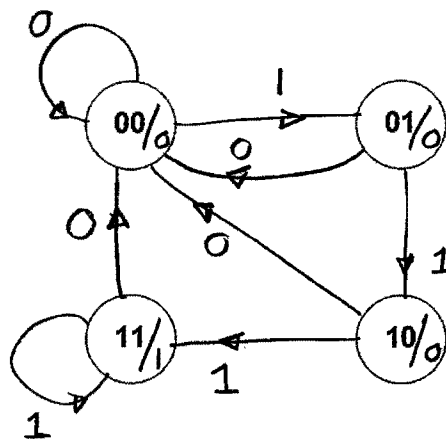
- b. Is the circuit Mealy or Moore?

Moore

- c. Use your answer in (a) above to complete the following two-dimensional table state table that gives the next state AB and the external output Y in terms of the present state AB and the external input X.

Present State AB	Next State AB		Output Y	
	X = 0	X = 1	X = 0	X = 1
00	00	01	0	0
01	00	10	0	0
10	00	11	0	0
11	00	11	1	1

- d. From the state table in c above, complete the state diagram shown below, indicating all state transitions and output values. States are given in the format AB.



- e. What is the minimum number of clock pulses required to move the circuit from state AB = 11 to state AB = 10?

3 clock cycles

- f. To satisfy the requirement in (e) above, the input X should have the sequence 0, 1, 1.

Question 5.

(25 Points)

A synchronous sequential circuit has a single input x and two outputs $Z_2 Z_1$. The state transition table of this circuit is given below (same table in 2 different forms).

Present State $y_1 y_0$	x	Next State	Outputs ($Z_2 Z_1$)
0 0	0	0 0	1 1
0 0	1	0 1	1 0
0 1	0	1 0	0 1
0 1	1	1 1	0 0
1 0	0	0 1	1 0
1 0	1	1 1	1 0
1 1	0	0 1	0 0
1 1	1	1 1	0 0

Present State $y_1 y_0$	Next State		Outputs ($Z_2 Z_1$)	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	0 0	0 1	1 1	1 0
0 1	1 0	1 1	0 1	0 0
1 1	0 1	1 1	0 0	0 0
1 0	0 1	1 1	1 0	1 0

- 8 a. Provide a minimized design for this circuit using gates and D Flip-Flops,
 3 b. Draw the logic diagram of the circuit.
 2 c. Classify each of the two outputs ($Z_2 Z_1$) either as Moore type or Mealy type.
 d. If this synchronous sequential circuit is implemented using a single ROM and a single register:
- Define the size of the required ROM, and its total capacity in bits.
 - What is the size of the register in bits?
 - Define the ROM Truth Table.
 - Draw the block diagram of this implementation (**CLEARLY LABEL each element, its inputs and outputs and show how they are connected**)

a) 4 states $\Rightarrow$ 2 FFs

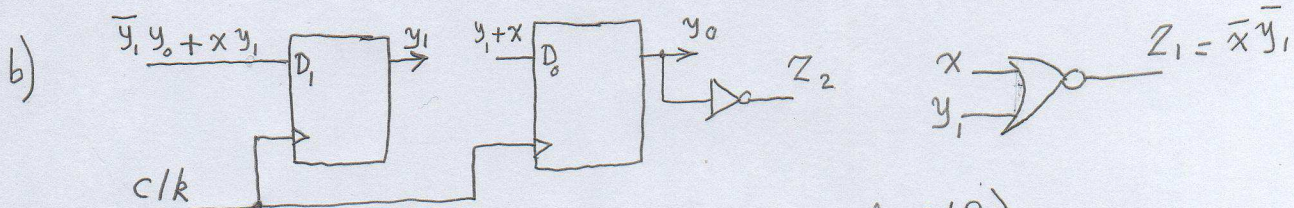
x	0	1	$y_1 y_0$	x	0	1	$y_1 y_0$	x	0	1	$y_1 y_0$	x	0	1	$y_1 y_0$
	0	0	0 0		0	1	0 0		1	1	0 0		1	0	0 0
	1	1	0 1		0	1	0 1		0	0	0 1		1	0	0 1
	0	1	1 1		1	1	1 1		0	0	1 1		0	0	1 1
	0	1	1 0		1	1	1 0		1	1	1 0		1	1	1 0

$$D_1 = \bar{y}_1 y_0 + x y_1$$

$$D_0 = y_1 + x$$

$$Z_2 = \bar{y}_0$$

$$Z_1 = \bar{y}_1 \bar{x}$$



c) $Z_1 = \bar{y}_1 \bar{x} \Rightarrow$ Mealy (depends on external I/Os)
 $Z_2 = \bar{y}_0 \Rightarrow$ Moore (independent of // //)

Present State y ₁ y ₀	x	Next State	Outputs (Z ₂ Z ₁)
0 0	0	0 0	1 1
0 0	1	0 1	1 0
0 1	0	1 0	0 1
0 1	1	1 1	0 0
1 0	0	0 1	1 0
1 0	1	1 1	1 0
1 1	0	0 1	0 0
1 1	1	1 1	0 0

Present State y ₁ y ₀	Next State		Outputs (Z ₂ Z ₁)	
	x = 0	x = 1	x = 0	x = 1
0 0	0 0	0 1	1 1	1 0
0 1	1 0	1 1	0 1	0 0
1 1	0 1	1 1	0 0	0 0
1 0	0 1	1 1	1 0	1 0

d. If the previous synchronous sequential circuit is implemented using a **single ROM** and a **single register**:

- 3 i. Define the size of the required ROM, and its total capacity in bits.
- 1 ii. What is the size of the register in bits?
- 3 iii. Define the ROM Truth Table.
- 5 iv. Draw the block diagram of this implementation (**CLEARLY LABEL each element, its inputs and outputs and show how they are connected**)

(i) Address I/P = y_1, y_0 , and $x \Rightarrow \# \text{ of locations (words)} = 2^3 = 8$
 size in bits of every location (word) = $y_1^+, y_0^+, Z_2, Z_1 = 4\text{-bits}$

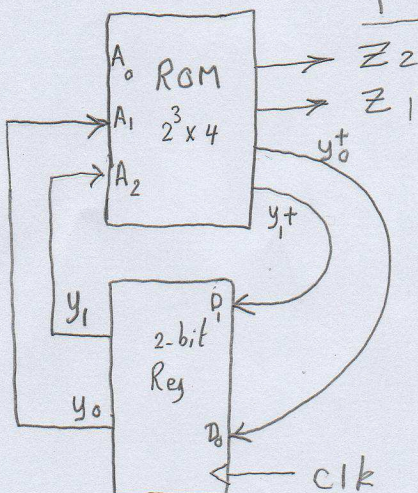
$$\text{Capacity (ROM)} = 2^3 \times 4 = 32\text{-bits}$$

(ii) size of Reg = # of state variables = 2-bits

(iii) ROM Table

Address			Storage			
y ₁	y ₀	x	y ₁ ⁺	y ₀ ⁺	Z ₂	Z ₁
0	0	0	0	0	1	1
0	0	1	0	1	1	0
0	1	0	1	0	0	1
0	1	1	1	1	0	0
1	0	0	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	1	0	0
1	1	1	1	1	0	0

(iv)



Question 6.

(6 Points)

A sequential circuit has 2 inputs x and y and an output Z . The output equals "1" when it receives 4th occurrence of equal inputs $x = y$ (not necessarily consecutive). After receiving these occurrences, the circuit starts counting these occurrences over again. The circuit has an additional reset input R which resets the circuit into the initial state.

$x = 0 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0$
 $y = 1 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1$
 $Z = 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0$

Draw the Mealy state diagram of the circuit

