KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 200 Fundamentals of Computer Engineering
Term 001 Lectures

	Date	Topics	Ref.
1	M 4/9	Syllabus. Introduction. Digital systems, Introduction to Computer Organization.	1.1
2	W 6/9	***Number systems:*** Binary, octal and hexadecimal numbers, number base conversion.	1.2, 1.3
3	S 9/9	Binary Codes, Binary Arithmetic. Representation of signed numbers: sign-magnitude, 1`s complement, and 2`s complement.	1.3, 1.4, handout
4	M 11/9	Signed Binary Addition and Subtraction.	3.9, 3.10, handout
5	W 13/9	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra.	2.1, 2.2
6	S 16/9	Boolean functions, Algebraic manipulation, Complement of a function.	2.2
7	M 18/9	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.	2.3
8	W 20/9	***Map method of simplification***: Two-, Three-, and Four-variable K-Map.	2.4
9	S 23/9	***Map manipulation:*** Essential prime implicants, Nonessential prime implicants, Simplification procedure.	2.4
10	M 25/9	Don`t care conditions. Simplification with Don`t care conditions.	2.5
11	W 27/9	Product-of-Sums Simplification, Five- and Six-variable K-map.	2.5, handout
12	S 30/9	***Nand and NOR gates:*** 2-level implementation.	2.6
13	M 2/10	***Nand and NOR gates:*** Multi-level implementation.	2.6
14	W 4/10	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Parity generation and checking.	2.7
15	S 7/10	***Combinational logic Design:*** Design Hierarchy, Top-Down Design, Analysis Procedure.	3.1, 3.2, 3.3
16	M 9/10	***Combinational logic Design:*** Design Procedure, Code Converters.	3.4
17	W 11/10	Magnitude Comparator Design. **(EXAM I)**	Handout
18	S 14/10	Decoders. Function implementation using decodres. Encoders: Priority Encoders.	3.5, 3.6

19	M 16/10	Multiplexers and Demultiplexers. Function implementation using multiplexers.	3.7
20	W 18/10	***Timing Analysis:*** Propagation Delays, Gate Delays, Rise and Fall Delays, Pulse Propagation, Inertial Delay.	Handout
21	S 21/10	***Binary Adders:*** Ripple Carry Adder, Carry Look-Ahead Adder.	3.8
22	U 22/10	Binary Subtraction, Binary Adders/Subtractors.	3.9, 3.10
23	S 28/10	BCD Adder, Binary Multiplier.	3.11, 3.12
24	M 30/10	***Sequential Circuits:*** Latches, SR and D-latch, Clocked latch.	4.1, 4.2
25	W 1/11	***Flip-Flops:*** Master-Slave, Edge-Triggered.	4.3
26	S 4/11	***Flip-Flops Characteristic Tables:*** D-FF, SR-FF, JK-FF, T-FF.	4.3
27	M 6/11	***Sequential Circuit Analysis:*** Input equations, State table.	4.4
28	W 8/11	***Sequential Circuit Analysis:*** State diagram, Mealy and Moore Models, Synchronizing Sequence.	4.4
29	S 11/11	Setup, Hold, Enable times. Timing control and Clocks. Path delay constraints, Clock signal design.	Handout
30	M 13/11	***Sequential Circuit Design:*** Design procedure, Construction of state diagrams and state tables.	4.5, handout
31	W 15/11	Designing with D-FFs. Designing with unused states. **(EXAM II)**	4.6
32	S 18/11	Designing with JK-FFs, Flip-Flop Excitation Tables.	4.7
33	M 20/11	Sequential Circuit Design Examples.	Handout
34	W 22/11	Sequential Circuit Design Examples.	Handout
35	S 25/11	State Reduction and State Assignment.	Handout
36	M 27/11	Registers, Registers with parallel load, Shift Registers.	5.2, 5.3
37	W 29/11	Serial addition, Shift register with parallel load, Bi-directional shift register.	5.3
38	S 2/12	***Ripple Counters:*** Up-Down Counters.	5.4
39	M 4/12	***Synchronous Binary Counters:*** Counters with JK-FF, Counters with D-FF.	5.5
40	W 6/12	Serial and Parallel Counter, Up-Down Binary Counter, Binary Counter with Parallel Load.	5.5
41	S 9/12	Other Counters: BCD Counter, Arbitrary Count Sequence.	5.6
42	M 11/12	***Memory and Programmable Logic Devices:*** Read-Only Memory.	6.1, 6.7
43	W 13/12	Combinational Circuit Implementation with ROM.	6.7
44	M 1/1	Programmable logic Array, Programmable Array logic.	6.8, 6.9
45	W 3/1	Final Exam Review	