***King Fahd University of Petroleum and Minerals***

***College of Computer Science and Engineering***

***Computer Engineering Department***

**COE 202: Digital Logic Design (3-0-3)**

**Term 162 (Winter 2016)**

**Major Exam 2**

**Saturday, April 29th, 2017**

**Time: 120 minutes, Total Pages: 9**

**Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_\_**

**Notes:**

Do not open the exam book until instructed

**Calculators are not allowed** (*basic, advanced, cell phones, etc*.)

Answer all questions

All steps must be shown

***Solution***

Any assumptions made must be clearly stated

Clearly label all inputs and outputs of any circuit component

|  |  |  |
| --- | --- | --- |
| **Question** | **Maximum Points** | **Your Points** |
| **1** | **8** |  |
| **2** | **11** |  |
| **3** | **4** |  |
| **4** | **12** |  |
| **5** | **8** |  |
| **6** | **7** |  |
| **7** | **8** |  |
| **Total** | **58** |  |

**Question 1: (8 marks)**

1. **Show the binary representations of the signed numbers shown in the table below using 8-bits signed-magnitude, 1’s complement and 2’s complement representations (record your answers in the table below). (4 marks)**

|  |  |  |  |
| --- | --- | --- | --- |
| ***Number*** | ***Signed-magnitude*** | ***1’s complement*** | ***2’s complement*** |
| +19 | **00010011** | **00010011** | **00010011** |
| -36 | **10100100** | **11011011** | **11011100** |

1. **Perform the following operations on 6-bits signed numbers using 2’complement representation. Check for overflow and mark clearly any overflow occurrences. (4 marks)**

|  |  |
| --- | --- |
| (1) 011001 + 110010  11  011001 (+25)  + 110010 (-14)  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  1 001011 (+11)  Overflow? (NO) | (2) 001110 – 100010 **= 001110 + 011110**  01  001110 (+14)  **+** **011110** (- - 30)  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  101100 (-20)  Overflow? (YES) |

**Question 2. (11 marks)**

# **For the following Boolean function shown in the K-map below:**

# **F(A, B, C, D)=m(0, 1, 2, 4, 5, 7, 8, 10, 11, 12, 13, 14, 15)**

AB

CD

00

01

11

10

00

01

11

10

1

1

0

1

1

1

1

0

1

1

1

1

1

0

1

1

1. **Identify all the *prime implicants* and the *essential prime implicants* of F. (6 marks)**

**Prime Implicants**: A' C', B C', B D, A C, C' D', A B, A D', B' D'

**Essential Prime Implicants**: A' C', B D, A C, B' D'

1. **Simplify the Boolean function F into a minimal sum-of-products expression. (2 marks)**

**F =** A' C' + B D + A C + B' D' + A B

OR **F =** A' C' + B D + A C + B' D' + C' D'

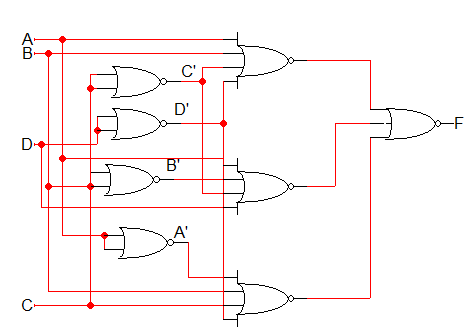
OR **F =** A' C' + B D + A C + B' D' + B C'

OR **F =** A' C' + B D + A C + B' D' + A D'

1. **Implement the function F using only NOR gates with minimum number of NOR gates. (3 marks)**

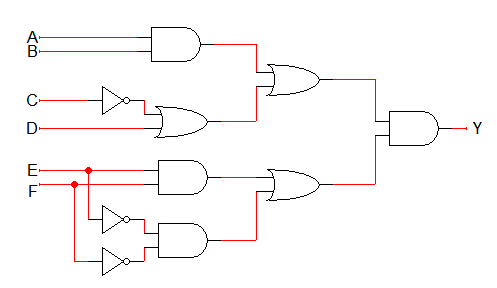
**F' =** A' B' C D + A' B C D' + A B' C' D

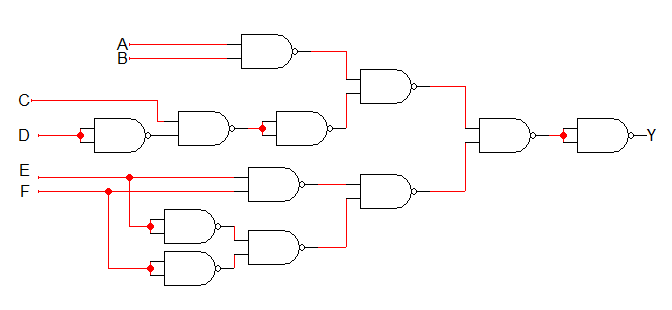
* **F = (A + B + C' + D') (A + B' + C' + D) (A' + B + C + D')**



# **Question 3:** **(4 marks)**

# **Convert the circuit below to 2-input NAND gates only. Redraw the circuit to obtain a multi-level NAND circuit implementation. Assume that only the true form of each input variable is available. Use the given circuit structure as is and do not attempt to simplify it.**

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**Question 4:** **(12 marks)**

# **It is required to design a circuit that receives a 3-bit signed number in 2's complement representation, X, and computes the equation Y = 3\*X – 2.**

1. **Determine the number of bits needed for the output Y. Justify your answer. (2 marks)**

The smallest negative value is -4. Thus, 3\*-4 -2 = -14. This implies that we need **5 bits** to represent the output correctly.

1. **Derive the truth table for the circuit. (5 marks)**

|  |  |  |
| --- | --- | --- |
| X2 X1 X0 | Y4 Y3 Y2 Y1 Y0 | Decimal Value |
| 0 0 0 | 1 1 1 1 0 | -2 |
| 0 0 1 | 0 0 0 0 1 | +1 |
| 0 1 0 | 0 0 1 0 0 | +4 |
| 0 1 1 | 0 0 1 1 1 | +7 |
| 1 0 0 | 1 0 0 1 0 | -14 |
| 1 0 1 | 1 0 1 0 1 | -11 |
| 1 1 0 | 1 1 0 0 0 | -8 |
| 1 1 1 | 1 1 0 1 1 | -5 |

1. **Derive the equation for the least significant output Y0 into a minimal sum-of-products expression. (3 marks)**

**Y0=X0**

1. **If the output of the circuit Y is fed as input to another circuit that will compute the equation Z = Y2, what will be the don't care conditions for Z. (2 marks)**

The don’t care conditions include all the values that do not occur at the output of Y, i.e. 0, +2, +3, +5, +6, +8 to +15, -1, -3, -4, -6, -7, -9, -10, -12, -13, -15, -16

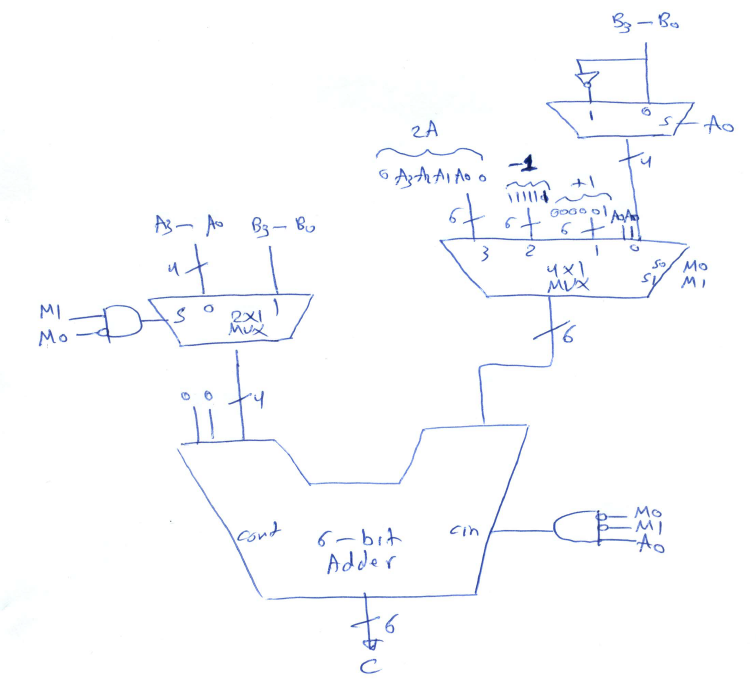
**Question 5:** **(8 marks)**

**It is required to design a 4-bit arithmetic Unit circuit with two 4-bit unsigned data inputs A and B, and two control inputs M1 and M0 and produce output C according to the following table:**

|  |  |  |  |
| --- | --- | --- | --- |
| ***M1*** | ***M0*** | ***Function Description*** | ***F(A, B)*** |
| 0 | 0 | If A is even, then C=A+B, else C=A-B | If A is even then C 🡨A+B; else C 🡨 A-B |
| 0 | 1 | Increment A | C 🡨 A + 1 |
| 1 | 0 | Decrement B | C 🡨 B – 1 |
| 1 | 1 | Multiply A by 3 | C 🡨 A x 3 |

**Design this circuit with minimum number of standard components (MUX, Decoders, Adders, Comparators, Logic Gates …etc.).**

**Properly label all components, their inputs and outputs.**



**Question 6: (7 marks)**

1. **Consider the combinational circuit shown with inputs X, Y, Z, and W, and outputs A, A\_b and B :**

*X*

*Y*

*X*

*Z*

***A\_b***

*W*

***B***

***A***

**Assuming that all input/output ports have been declared properly; Write Verilog *assign* statement(s) to describe the circuit above (including worst case delays of the outputs).**

**Outputs *A\_b* and *B* should be expressed as functions of the output *A* and other inputs.**

**Assume the following gate delays; inverter’s delay= 1 (time unit), AND’s delay= 2, and**

**OR’s delay=3. (4 marks)**

**assign #5 A = X & Y | X & Z ;**

**assign #1 A\_b = ~A ;**

**assign #2 B= A & W :**

1. **Write a parametrized *behavioral* Verilog description of a circuit that takes an *n-*bit signed number input *A* represented in 2’s complement and produce its absolute value Y=|A| at the output. (3 marks)**

**module ABS\_Val #(parameter n=8)**

**(input [n-1:0] A, output wire [n-2:0] Y);**

**assign Y = A[n-1] ? –A : A ;**

**// or assign Y = A[n-1] ? (1+~A[n-1:0]) : A ;**

**endmodule**

**Question 7: (8 marks)**

1. **Given implement** **F** **using minimum number of 2-to-4 decoders and a single logic gate with minimum number of inputs. Clearly label all your circuit components, their inputs and their outputs.**  **(5 marks)**

**Note that we do not need minterms m4-m11, so we are not going to generate them!**

**I0**  **m0**

**I1**  **m1**

**m2**

**En**  **m3**

**I0**  **m0**

**I1**  **m1**

**m2**

**En**  **m3**

**I0**  **m12**

**I1**  **m13**

**m14**

**En**  **m15**

**B A**

**D C**

**D C**

**1**

**F**

1. **Given , implement F using a single *minimum size Multiplexor*. Assume inputs are available in true and complement form. Clearly label all your circuit components, their inputs and their outputs. (3 marks)**

**S1S0**

**D0**

**D1**  **D2**

**D3**

**F**

**C’ C C C**

**A B**

|  |  |  |
| --- | --- | --- |
| **A B C** | **F** |  |
| **0 0 0** | **1** | **C’** |
| **0 0 1** | **0** |
| **0 1 0** | **0** | **C** |
| **0 1 1** | **1** |
| **1 0 0** | **0** | **C** |
| **1 0 1** | **1** |
| **1 1 0** | **0** | **C** |
| **1 1 1** | **1** |