King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)

Term 121 (Fall 2012)

Major Exam II

Thursday Nov. 22, 2012

Time: 150 minutes, Total Pages: 9

Name:________________________________ ID:______________ Section: _______

Notes:

- Do not open the exam book until instructed
- **Calculators are not allowed** (*basic, advanced, cell phones, etc.*)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	15	
2	14	
3	9	
4	15	
5	11	
6	13	
7	8	
Total	85	

Question 1. **(15 points)**

The logic function F(W,X,Y,Z) is plotted on the K-map shown below. Z is the LSB. **(15 Points)**

WX \ YZ	00	01	11	10
00			1	
01	1		1	1
11			1	
10	1	1	1	

a. The function F can be expressed in the canonical form as a product of maxterms as follows: **(2 points)**

F (W,X,Y,Z) = Π M (______________________________________)

b. Indicate whether each of the following is True or False: **(2 Points)**

- $W\overline{X}Z$ is a prime implicant for the function
- $\overline{W}XY$ is an essential prime implicant for the function

c. The function F can be minimized to an optimal algebraic sum of products as: **(3 points)**

F (W,X,Y,Z) = ____

d. The function F can be minimized to an optimal algebraic product of sums as: **(5 points)**

F (W,X,Y,Z) = ____

e. If we are told that we should not care about the output of the circuit implementing F for the input combination WXYZ = 1010. **(3 Points)**

i) Indicate this condition on the K-map

ii) If this information leads to a more optimal expression for F than that obtained in part (c) above, then give that more optimal expression.

Question 2. **(14 Points)**

We would like to design a combinational circuit that multiples two unsigned integers X and Y and produces the product as output Z, i.e. Z = XY. Each of the two integers X and Y is 2 bits. The binary representations of the input and output numbers are X_1 X_0 for X (X_0 is the LSB), Y_1 Y_0 for Y (Y_0 is the LSB), $Z_n \ldots Z_2Z_1Z_0$ for Z (Z_0 is the LSB).

a. **(8 points)** Fill in all the required information in the table below.

Circuit Input X_1 X_0 Y_1 Y_0	Circuit Output $Z_n \ldots Z_2Z_1Z_0$	
(Binary)	(Binary)	(Decimal)

b. **(6 points)** Use a K-map of the appropriate size to minimize the binary output **Z1** and express the minimized function as a <u>sum of products</u> in terms of the binary inputs X_1, X_0, Y_1, and Y_0. Show all your work.

Question 3. **(9 Points)**

(a) (**5 points**) Draw the multi-level **NAND** logic diagram for the following Boolean expression, ***don't simplify***:

$$(\overline{A}B + \overline{C}D)E + A\overline{D}(B + C)$$

(b) (**4 points**) Using the **minimum** number of logic gates, draw the 2-level **NOR** logic diagram for the following Boolean expression:

$F(A,B,C) = \Sigma m(0, 3, 5, 6)$

Question 4. **(15 Points)**

(a) **(6 points)** Determine the decimal value of the **7-bit** binary number (1001100) when interpreted as:

Unsigned number	Signed-magnitude number	Signed-1's complement number	Signed-2's complement number

(b) **(3 points)** Find the **smallest** 7-bit signed-2's complement number that can be added to the 7-bit signed-2's complement number (1001100) **without causing an overflow**. Note that negative numbers are considered to be smaller than positive numbers.

(c) **(6 points)** Perform the following **signed-2's complement arithmetic** operations in binary using **5 bits**. All numbers given are represented in the signed-2's complement notation. Indicate clearly the carry values out of the last two bits. For each of the two operations, check and indicate whether an overflow has occurred or not.

Operation	Carry value out of the 4th bit	Carry value out of the 5th bit	Overflow occurred? (Yes/No)
a. 01011 +11110			
b. 01001 -10010			

Question 5. **(11 Points)**

(a) **(6 points)** You are given **one 3-to-8 decoder**, **one NOR** gate and **one OR** gate to implement the two functions given below.

$$F_1(A,B,C) = \Pi M(0, 1, 4, 5, 6)$$
$$F_2(A,B,C) = \sum m(0, 4, 6) + \sum d(1, 3)$$

Draw the circuit and properly label all input and output lines.

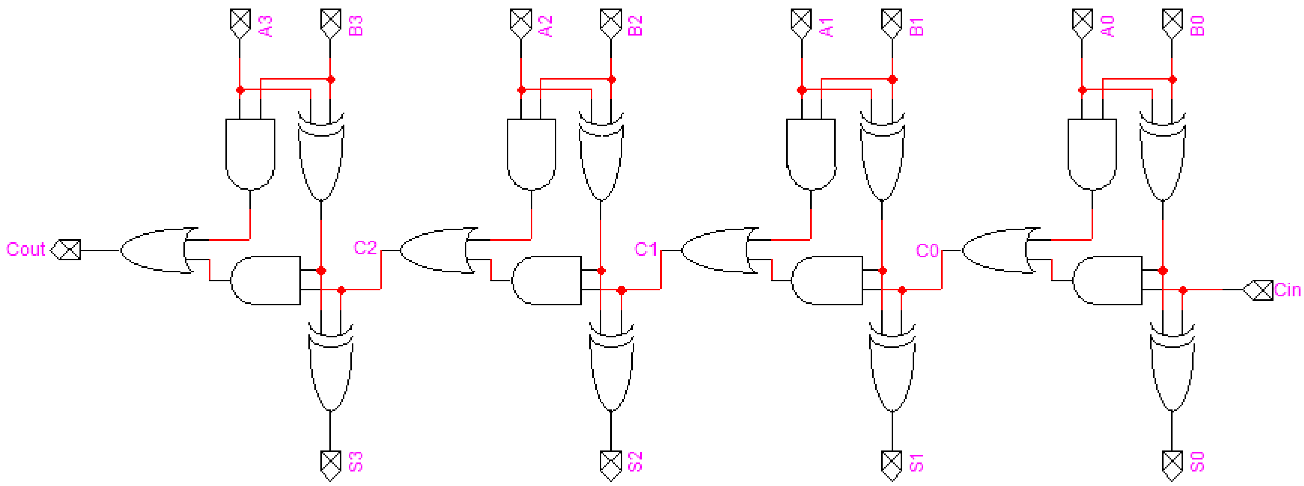
(b) **(5 points)** Given the truth table below for a function with four inputs (A, B, C and D) and one output F, implement F using a 4-to-1 MUX (with 2 select lines) and additional logic. Show how you obtained your solution, and properly label all input and output lines. Apply A and B to the select inputs.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Question 6. **(13 points)**

Assume that the delay of a 2-input XOR gate is 3ns while the delay of other gates is equal to the gate's number of inputs, i.e. the delay of an inverter is 1ns, the delay of a 2-input AND gate is 2ns, the delay of a 2-input OR is 2ns, the delay of a 3-input AND gate is 3ns, the delay of a 3-input OR gate is 3ns, etc.

(a) **(6 points)** A 4-bit **Ripple Carry Adder** (RCA) is given below:



Determine and compute the **longest delay** in the **4-bit Ripple Carry Adder** (RCA).

(b) **(4 points)** Show the design of a **2-bit Carry Look-Ahead Adder** (CLA) by drawing its logic diagram.

(c) **(3 points)** Using the delay assumptions given in the beginning of the question, determine and compute the **longest delay** in the **2-bit Carry Look-Ahead Adder** (CLA).

Question 7. **(8 points)**

Using a **minimal** number of **MSI** components such as: **decoders, encoders, multiplexers, adders, magnitude comparators** and other necessary logic gates, design a circuit that takes two **4-bit** binary numbers $\boldsymbol{A=A_3A_2A_1A_0}$ and $\boldsymbol{B= B_3B_2B_1B_0}$ and a 2-bit user selection input $\boldsymbol{S=S_1S_0}$. The circuit should produce a 5-bit output $\boldsymbol{O= O_4O_3O_2O_1O_0}$ according to the following table:

S_1S_0	*O* is equal to
00	A+B
01	A-B
10	A+1
11	2*A