King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 112 (Spring 2012)
Major Exam II
Thursday April 12, 2012

Time: 150 minutes, Total Pages: 13

Name:___KEY_____ ID:_____ Section: _____

Notes:

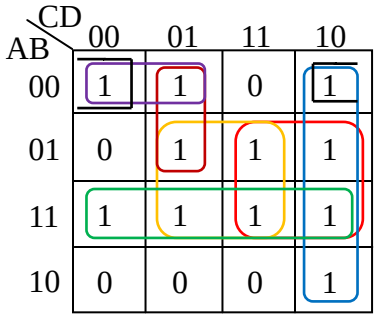
- Do not open the exam book until instructed
- **Calculators are not allowed** (*basic, advanced, cell phones, etc*.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	23	
2	22	
3	10	
4	20	
5	15	
6	15	
Total	105	

Question 1. **(23 points)**

(a) For the following Boolean function shown in the K-map:

$$F(A, B, C, D)=\Sigma\, m(0, 1, 2, 5, 6, 7, 10, 12, 13, 14, 15)$$



(i) Identify all the *prime implicants* and the *essential prime implicants* of F.

Prime Implicants:

$$A\,B, \quad C\,\overline{D}, \quad B\,C, \quad B\,D, \quad \overline{A}\;\overline{B}\;\overline{C}, \quad \overline{A}\;\overline{B}\;\overline{D}, \quad \overline{A}\;\overline{C}\,D$$

Essential Prime Implicants:

$$A\,B, \quad C\,\overline{D}$$

(ii) Simplify the Boolean function **F** into a minimal sum-of-products expression.

$$F = A\,B + C\,\overline{D} + B\,D + \overline{A}\;\overline{B}\;\overline{C}$$

(b) Consider the following Boolean function **F** together with the don`t care conditions **d** shown in the k-map:

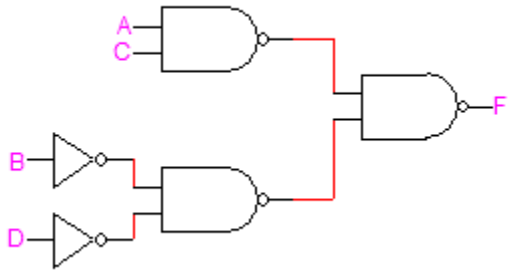
F(A, B, C, D)=Σ m(0, 10, 15), d(A, B, C, D)=Σ m(1, 2, 4, 8, 11, 14)

AB \ CD	00	01	11	10
00	1	X	0	X
01	X	0	0	0
11	0	0	1	X
10	X	0	X	1

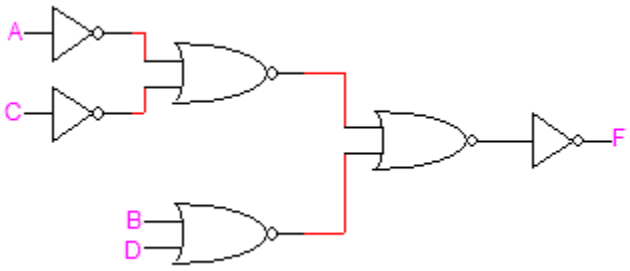
(i) Simplify the Boolean function **F** together with the don`t care conditions **d,** into <u>minimal</u> <u>sum-of-products</u> expression.

$$F = A\,C + \overline{B}\;\overline{D}$$

(ii) <u>Starting with the sum-of-products expression</u>, implement the function using only **NAND** gates and **Inverters**.



(iii) <u>Starting with the sum-of-products expression</u>, implement the function using only **NOR** gates and **Inverters**.



Question 2. **(22 Points)**

Design a circuit that accepts two 2-bit unsigned numbers A = A_1A_0 and B = B_1B_0. The circuit produces A – B when A > B, and produces A + B otherwise. Find the following:

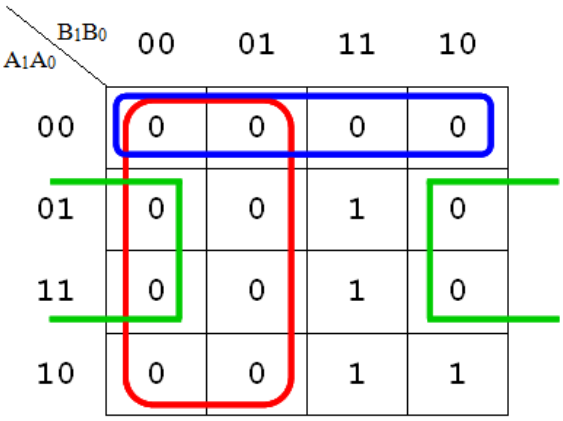
(a) The number of outputs produced by the circuit.

$A - B$ result is at most 2 bits, $A + B$ result is at most 3 bits $\Rightarrow$ **# outputs = 3**

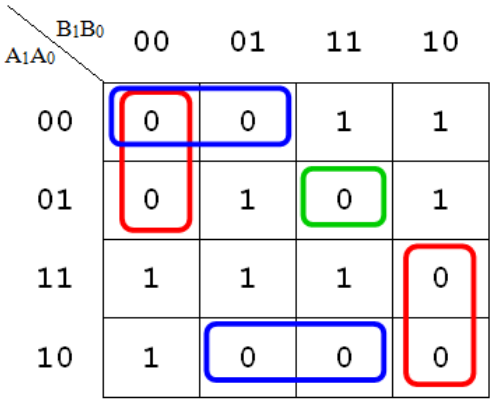
(b) The truth table of the circuit.

A_1	A_0	B_1	B_0	O_2	O_1	O_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	1	1	1	0

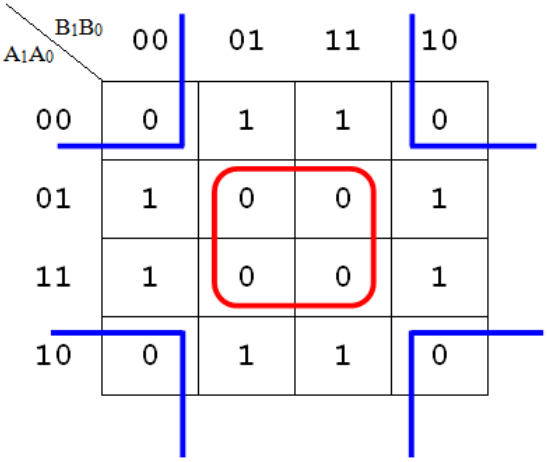
(c) The minimal <u>product-of-sums</u> expression for each output.



$$O_2 = (A_1 + A_0)(\overline{A_0} + B_0)B_1$$



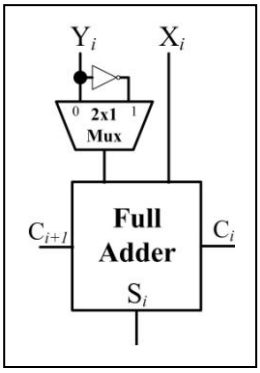
$$O_1 = (A_1 + A_0 + B_1)(A_1 + B_1 + B_0)(\overline{A_1} + A_0 + \overline{B_0})(\overline{A_1} + \overline{B_1} + B_0)(A_1 + \overline{A_0} + \overline{B_1} + \overline{B_0})$$



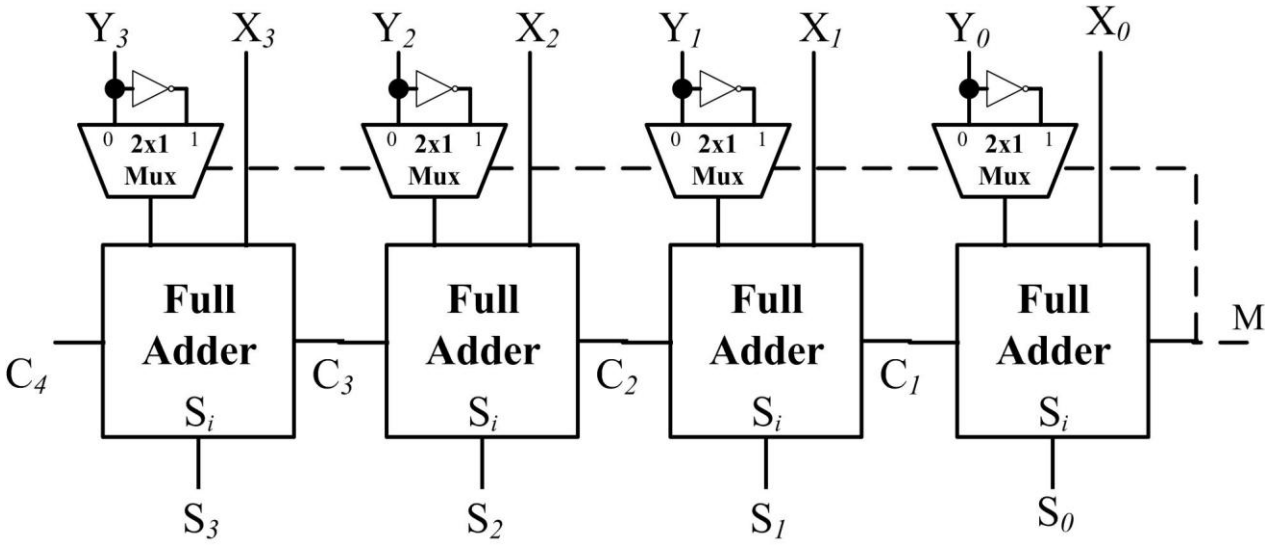
$$O_0 = (A_0 + B_0)(\overline{A_0} + \overline{B_0})$$

Question 3. **(10 Points)**

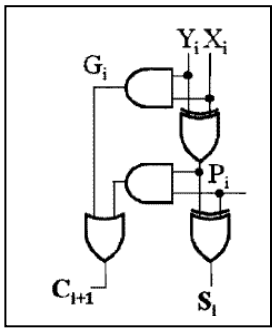
(a) Use the shown circuit on the right to build a 4-bit **adder-subtractor** which can add or subtract two 4-bit numbers X and Y. A mode control input signal **M** is used to define the operation to be performed; if **M=0**, output is (X+Y) while if **M=1**, output is (X-Y).



CLEARLY label ALL inputs and outputs



(b) The Full-Adder circuit is shown to the right. Given the following gate delays;



Gate/ Circuit	Propagation Delay
Inverter	**1 τ**
AND, OR	**2 τ**
XOR	**4 τ**
2x1 **Mux**	**5 τ**

(i) What is the carry propagation delay per Full adder stage?

$T(CP) = T_{AND} + T_{OR} = 4\tau$

(ii) For an ***n*-bit** Ripple-Carry **Adder-Subtractor** using the circuit of part (a), what is the total delay for the n^{th} sum bit and the $(n+1)^{th}$ carry-out bit?
(*Clearly identify each delay component*)

Delay of the n^{th} Sum output = $(1\tau+5\tau+4\tau+(n-1)*4\tau+4\tau) = 4n\tau+10\tau$
Delay of the $(n+1)^{th}$ Carry output = $(1\tau+5\tau+4\tau+(n)*4\tau) = 4n\tau+10\tau$

Question 4. **(20 Points)**

(a) If **6-bit registers** are used, show the binary number representation of the decimal numbers (+23), (–23), (+11), and (–11) using the following representation systems:

	+23	**–23**	**+11**	**–11**
Signed magnitude system	**010111**	**110111**	**001011**	**101011**
Signed 1's complement system	**010111**	**101000**	**001011**	**110100**
Signed 2's complement system	**010111**	**101001**	**001011**	**110101**

(b) Provide the decimal equivalent of each of the following **signed 2's complement** numbers:

Signed 2's Complement Number	**Equivalent Decimal Number**
001101	**+13**
010011	**+19**
101101	**-19**
110011	**-13**

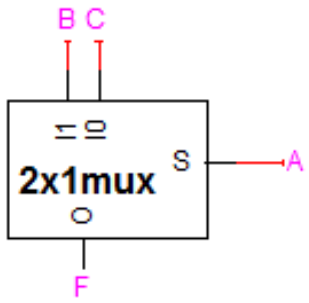
(c) If **6-bit registers** are used, perform the following **signed 2's complement** arithmetic operations on the provided signed 2's complement numbers. For each case, state whether the result is correct or an **overflow** has occurred.

Signed 2's Complement Arithmetic Operation	Correct Answer or Overflow?
(i) 001101 – 101101 001101 – 101101 ⇒ + 010011 100000	***Overflow***
(ii) 010011 – 001101 010011 – 001101 ⇒ + 110011 000110	***Correct***
(iii) 101101 + 110011 101101 + 110011 100000	***Correct***

Question 5. **(15 Points)**

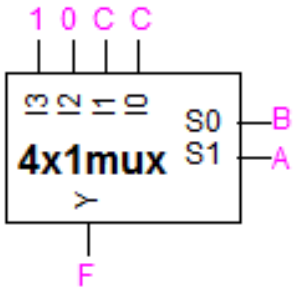
Given the function $F(A,B,C) = A\,B + \overline{A}\;C$

(a) Implement F using a single 2-to-1 MUX with no additional gates. Properly label all input and output lines.



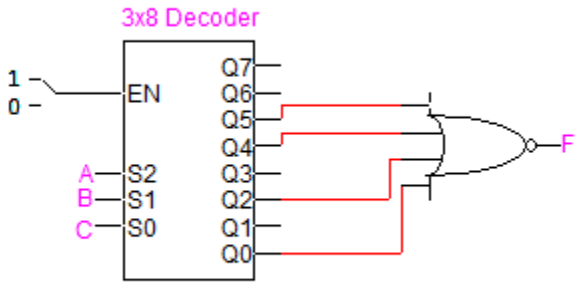
(b) Implement F using a 4-to-1 MUX. Properly label all input and output lines.

$F = \overline{A}\;\overline{B}\;(C) + \overline{A}\;B(C) + A\,\overline{B}\;(0) + A\,B\;(1)$

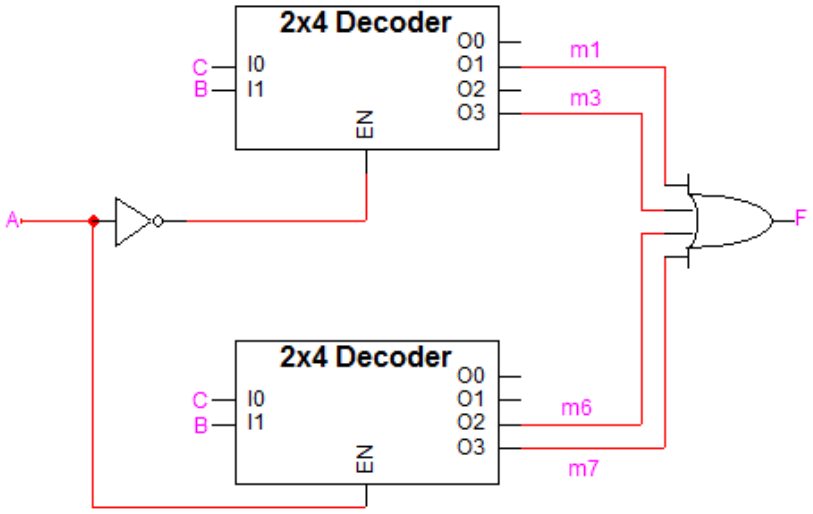


(c) Implement F using a single 3-to-8 decoder, and a single NOR gate. Properly label all input and output lines.

$F=\sum m(1,3,6,7)=\Pi M(0,2,4,5)$



(d) Implement F using two 2-to-4 decoders with enable, one inverter, and one OR gate. Properly label all input and output lines.



Question 6. **(15 points)**

(a) Given two 4-bit signed 1's complement numbers **A** and **B**; for A = 1010 and B = 1101;

(i) What are the corresponding decimal values of A and B?

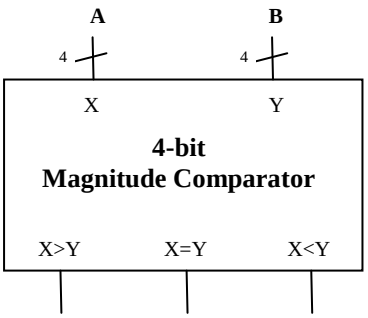
A=1010 = (-5)$_{Decimal}$ **B=1101 = (-2)$_{Decimal}$**

(ii) If these values of A and B are applied to the shown magnitude comparator circuit, what are the values of the resulting outputs?

(X > Y) = __0_____

(X = Y) = __0_____

(X < Y) = __1_____



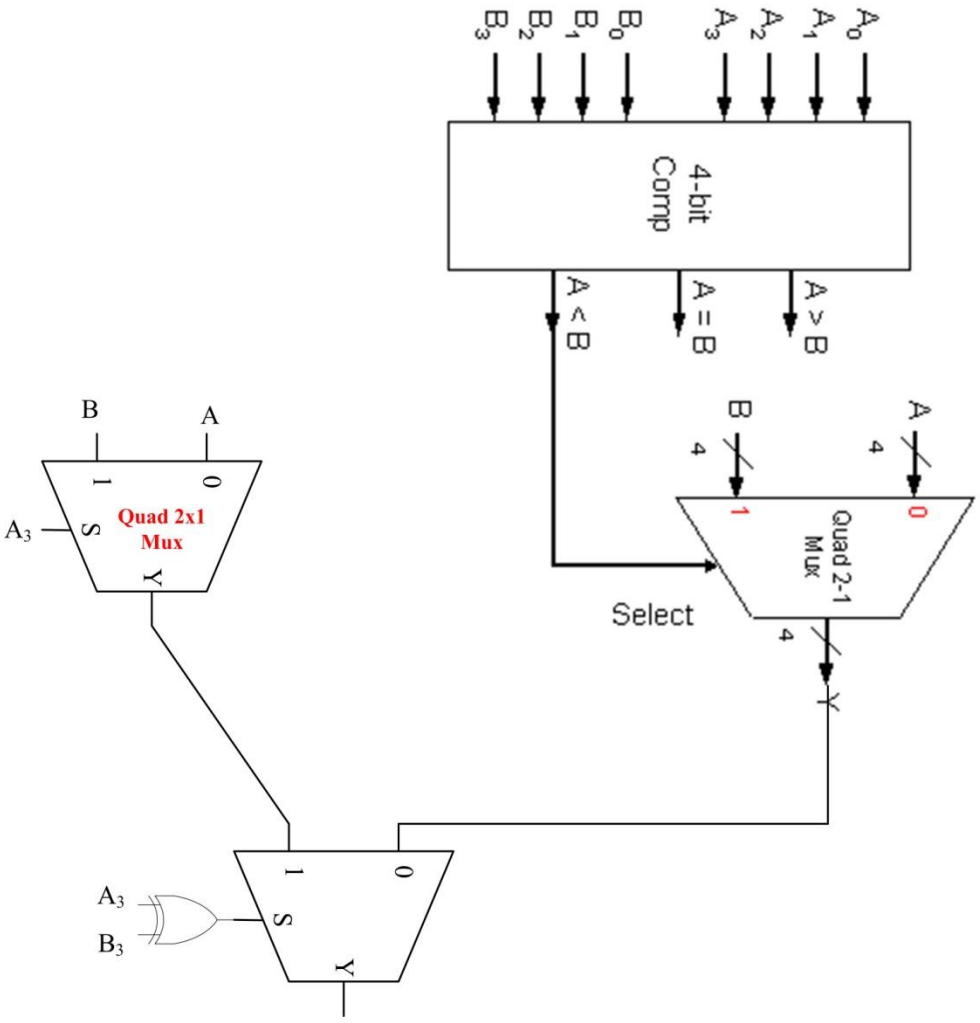
(b) Given two 4-bit signed 1's complement numbers **A** and **B**, design the following circuits using any number of the following components: XOR gates, decoders, encoders, multiplexers, adders, and/or magnitude comparators:

(i) A circuit whose 4-bit output **Z** equals the larger of either **A** or **B** given that both **A** and **B** are positive values.

(ii) A circuit whose 4-bit output **Z** equals the larger of either **A** or **B** given that both **A** and **B** are negative values (*Hint: use conclusions of part* (a)).

(iii) A circuit whose 4-bit output **Z** equals the larger value of either **A** or **B** given that **A** and **B** may be +ive or –ive in any possible combination.

(*You **must** clearly label the MSI parts used together with all inputs and outputs*)


B3 B2 B1 B0 A3 A2 A1 A0
4-bit Comp
A < B
A = B
A > B
B
A
4
4
1
0
Quad 2-1 Mux
Select
4
Y
B
A
1
0
A3
S
Quad 2x1 Mux
Y
A3
B3
1
0
S
Y