**Question 2:**

Design a circuit that accepts two 2-bit unsigned numbers *A* = *A*1*A*0 and *B* = *B*1*B*0. The circuit produces *A* – *B* when *A* > *B*, and produces *A* + *B* otherwise. Find the following:

1. **(2 points)** The number of outputs produced by the circuit.

*A* – *B* result is at most 2 bits, *A* + *B* result is at most 3 bits ⇒ **# outputs = 3**

1. **(8 points)** The truth table of the circuit.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *A*1 | *A*0 | *B*1 | *B*0 | *O*2 | *O*1 | *O*0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |

1. **(12 points)** The *minimal product-of-sums* expression for each output.

B1B0

A1A0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | **0** | **0** | **0** | **0** |
| **01** | **0** | **0** | **1** | **0** |
| **11** | **0** | **0** | **1** | **0** |
| **10** | **0** | **0** | **1** | **1** |



B1B0

A1A0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | **0** | **0** | **1** | **1** |
| **01** | **0** | **1** | **0** | **1** |
| **11** | **1** | **1** | **1** | **0** |
| **10** | **1** | **0** | **0** | **0** |



B1B0

A1A0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **00** | **01** | **11** | **10** |
| **00** | **0** | **1** | **1** | **0** |
| **01** | **1** | **0** | **0** | **1** |
| **11** | **1** | **0** | **0** | **1** |
| **10** | **0** | **1** | **1** | **0** |



**Question 4:**

1. **(12 points)** If 6-bit registers are used, show the binary number representation of the decimal numbers (+23), (–23), (+11), and (–11) using the following representation systems:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **+23** | **–23** | **+11** | **–11** |
| Signed magnitude system | **010111** | **110111** | **001011** | **101011** |
| Signed 1’s complement system | **010111** | **101000** | **001011** | **110100** |
| Signed 2’s complement system | **010111** | **101001** | **001011** | **110101** |

1. **(2 points)** Provide the decimal equivalent of each of the following signed **2’s complement** numbers:

|  |  |
| --- | --- |
| **Signed 2’s Complement Number** | **Equivalent Decimal Number** |
| **001101** | **+13** |
| **010011** | **+19** |
| **101101** | **-19** |
| **110011** | **-13** |

1. **(6 points)** If 6-bit registers are used, perform the following signed 2’s complement arithmetic operations on the provided signed 2’s complement numbers. For each case, state whether the result is ***correct*** or an ***overflow*** has occurred.

|  |  |
| --- | --- |
| **Signed 2’s Complement Arithmetic Operation** | **Correct Answer or Overflow?** |
| 1. **001101 – 101101**

 **001101 ⇒ 001101****– 101101 ⇒ + 010011**  **⇒ 100000** | ***Overflow*** |
| 1. **010011 – 001101**

 **010011 ⇒ 010011****– 001101 ⇒ + 110011**  **⇒ 000110** | ***Correct*** |
| 1. **101101 + 110011**

 **101101****+ 110011** **100000** | ***Correct*** |