King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 162 (Winter 2017)
Final Exam
Wednesday, May 24th, 2017

Time: 120 minutes, Total Pages: 10

Name:__KEY_____ ID:_____ Section: _____

Notes:
Do not open the exam book until instructed
Calculators are not allowed (*basic, advanced, cell phones, etc*.)
Answer all questions
All steps must be shown
Any assumptions made must be clearly stated

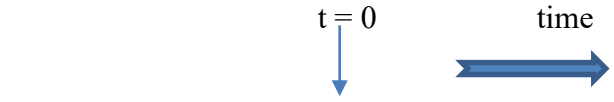
Question	Maximum Points	Your Points
1	6	
2	8	
3	10	
4	7	
5	9	
6	8	
7	13	

Total	61	

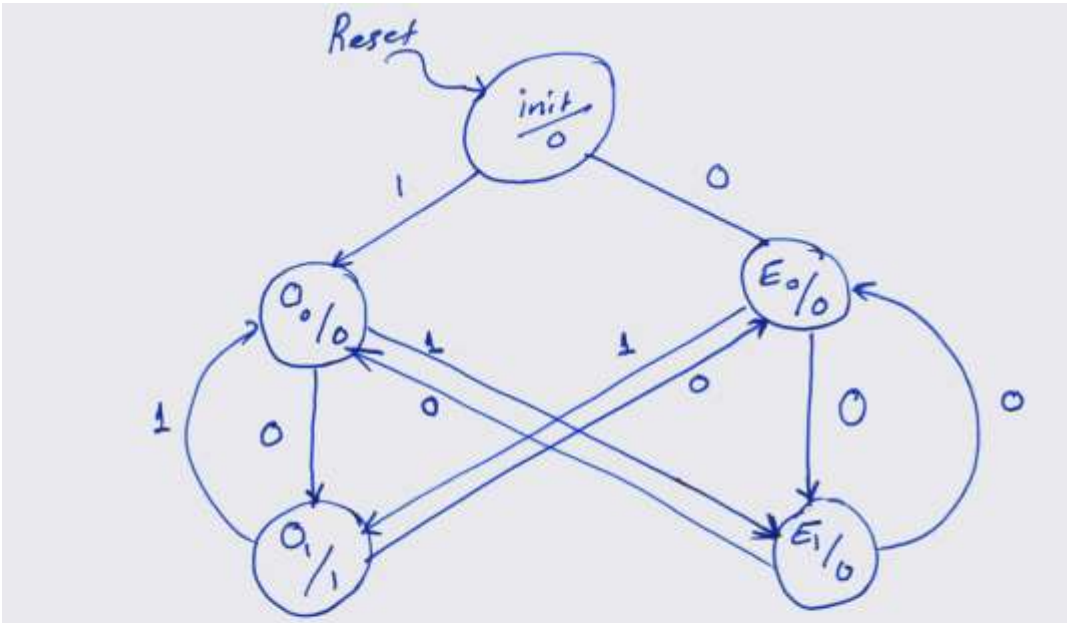
Question 1: **(6 points)**

A **Moore** *Odd parity detector* circuit has a single input ***x*** and a single output signal ***parity***. The input consists of 2-bit data chunks that are ***serially*** *received* at the input ***x***. The ***parity*** output is 1 whenever the received 2-bit stream has an odd number of 1's, and 0 otherwise. Draw the state diagram of this circuit. **The circuit has an asynchronous reset input to reset the machine to a reset state with an output of 0.** You are *only* required to draw the state diagram **Nothing MORE**)

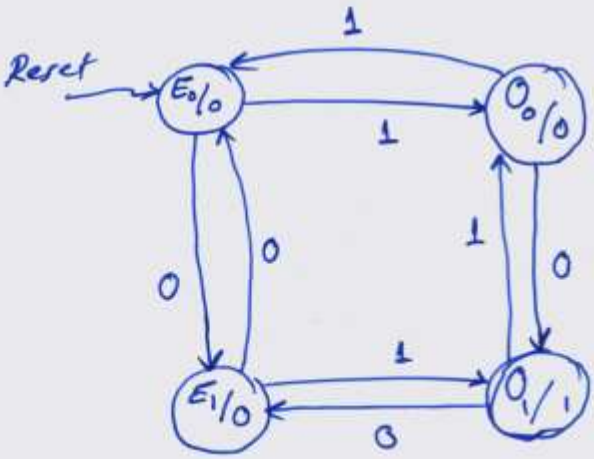
Example:



Input	***x***	1 1_1 0_0 0_0 1_0 0_1 0_
Output	***parity***	0 0_**0** 0_**1** 0_**0** 0_**1** 0_**0** 0_**1**

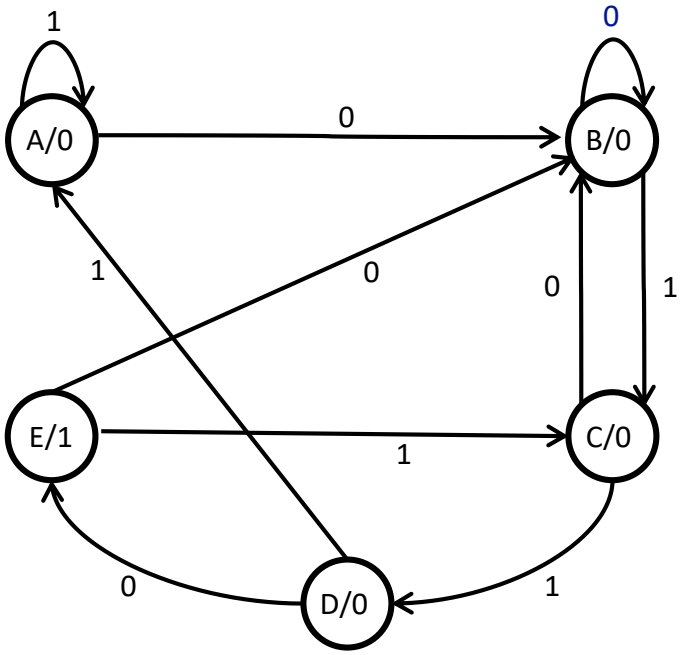


* Alternative Solution

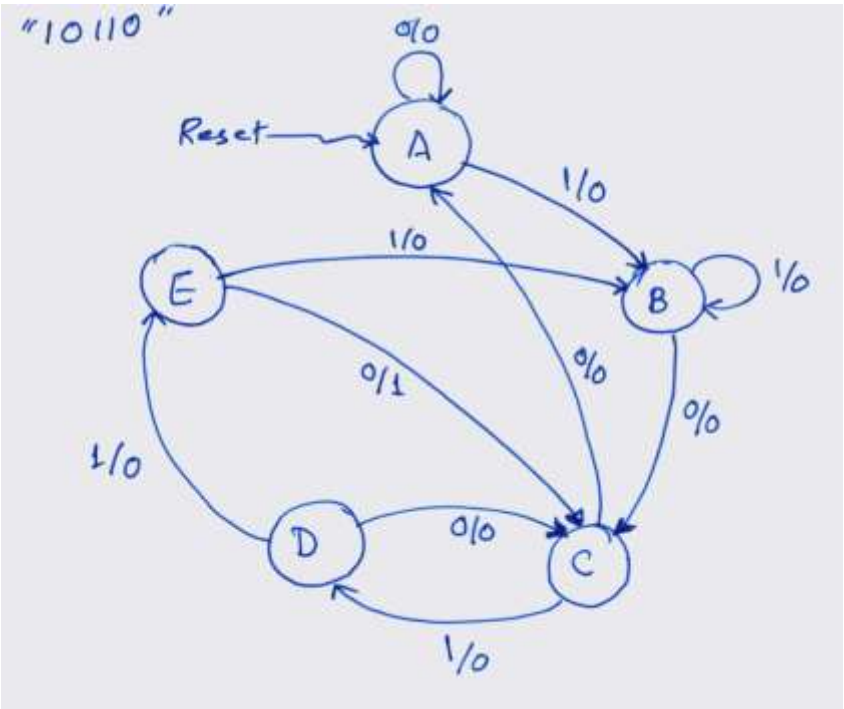


Question 2: **(8 points)**

1. The shown state diagram is for a **Moore** FSM of a sequence detector with a single input **X** and a single output **Y**. The circuit can detect overlapping (**overlapping**/non-overlapping) versions of the sequence **0110** (write the sequence). **(3 points)**



2. It is required to design a sequence detector that detects the sequence {10110} (i.e., 1 followed by 0 followed by 1 followed by 1 followed by 0) in a serial input **Z** and produces 1 at the output **W** when the sequence is detected. Assuming overlapping sequences derive the state diagram of the circuit assuming a **MEALY** model. Also, assume the existence of an asynchronous *reset* input to reset the circuit to a reset state. You are *only* required to draw the state diagram **Nothing MORE**.



(5 points)

Question 3: **(10 points)**

The state transition table below is for a sequential circuit with one input **X** and one output **Y**. The circuit has two state variables **A** and **B,** and an asynchronous input Reset that resets the circuit to state 00:

Reset State →

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A B	A^+ B^+	A^+ B^+	Y	Y
0 0	0 0	0 1	0	1
0 1	0 0	1 0	1	0
1 0	0 0	1 0	0	1
1 1	0 1	1 0	1	0

1. Does this circuit has any unused states? Briefly explain your answer **(2 points)**

   Yes, state 11, no normal input sequence can get the circuit to that state

2. Design the above circuit using minimum number of logic gates and D-FFs (with asynchronous reset inputs) and draw the logic diagram of the designed circuit. The circuit should have asynchronous reset that reset it to state 00 **(8 points)**

	00	01	11	10
0	0	1	? 3	2
1	4	1 5	? 7	1 6

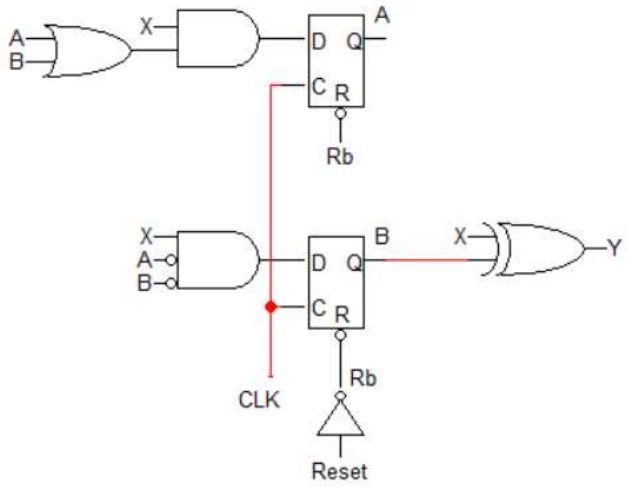
$D_A = X(A+B)$

	00	01	11	10
0	0	1	? 3	2
1	1 4	5	? 7	6

$D_B = XA'B'$

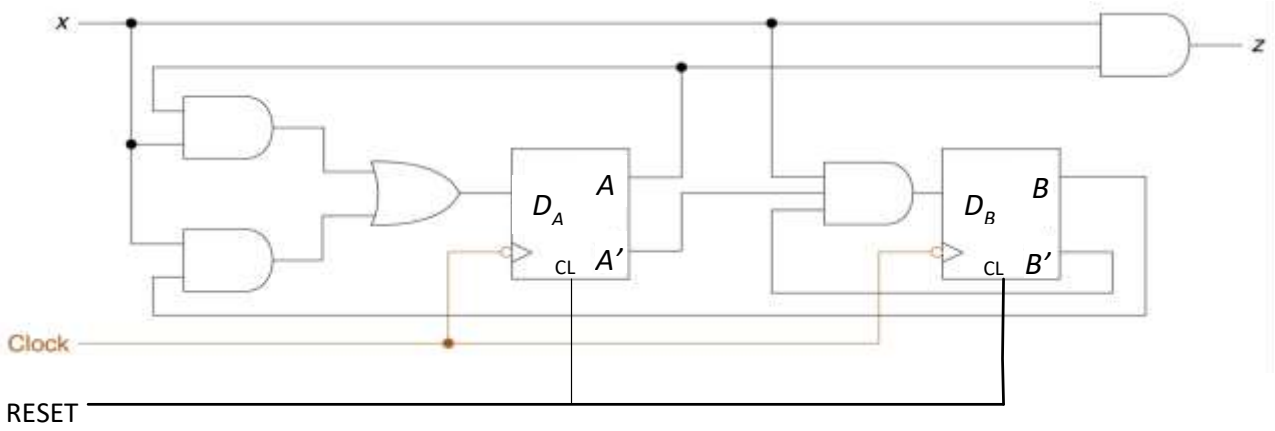
	00	01	11	10
0	0	1 1	? 3	2
1	1 4	5	? 7	1 6

$Y = X \oplus B$



Question 4: **(7 points)**

The sequential circuit shown below has a single input ***x*** together with a **RESET** input to initialize the circuit. The used D-FFs have direct/asynchronous Clear inputs (shown in the figure as CLR).



a. Obtain the Boolean expressions for the D_A , D_B (flip flop inputs) and the output ***z***. **(3 points)**

$D_A = (A + B)\,x$

$D_B = A'B'x$

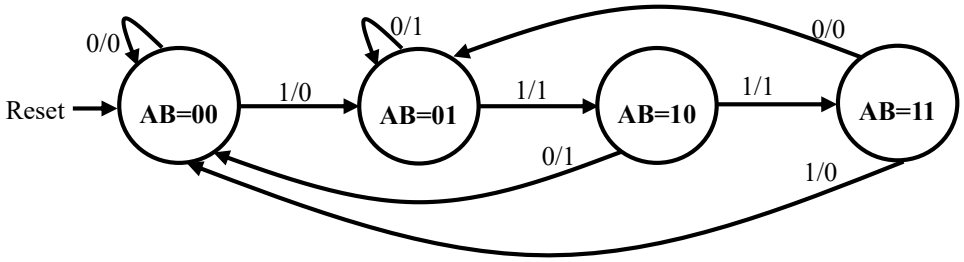
$z = Ax$

b. Derive the state transition table of the circuit (fill the table below). **(4 points)**

Present State		Input	Next State		Output
A	**B**	**x**	**A+**	**B+**	**z**
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	1	1	0	1

Question 5: **(9 points)**

The state diagram below is for a sequential circuit that one input **X** (in addition to an **asynchronous Reset** input), one output **Y,** and state variables **A** and **B**.



1. Obtain the state transition table of this circuit. (**2 points**)

A	*B*	*X*	*A+*	*B+*	*Y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	0	0	0

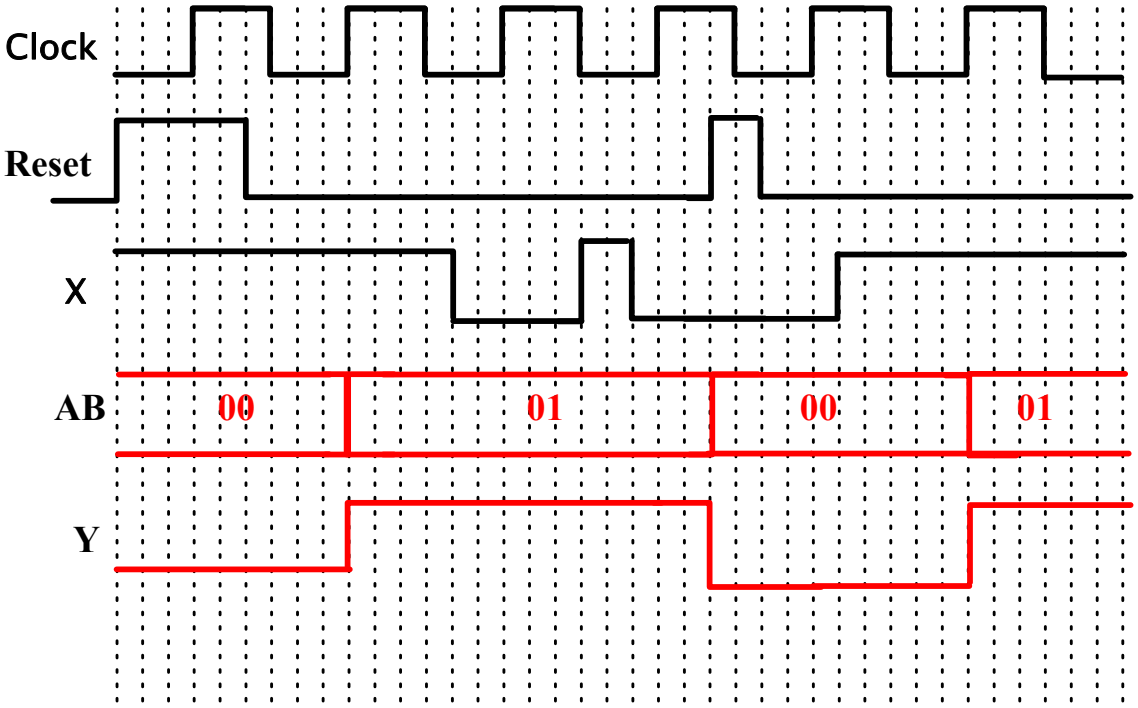
2. Specify whether this circuit is a Mealy or Moore Machine? Explain (**1 point**)

   Moore, the output in each and every state is constant (i.e. does not depend on the input)

3. If the circuit is in state **00**, what is minimum number of clock cycles required to reach state **11**?
   3 clock cycles (00→01→10→11) (**1 point**)

   What is the required input sequence? (**1 point**)
   1-1-1

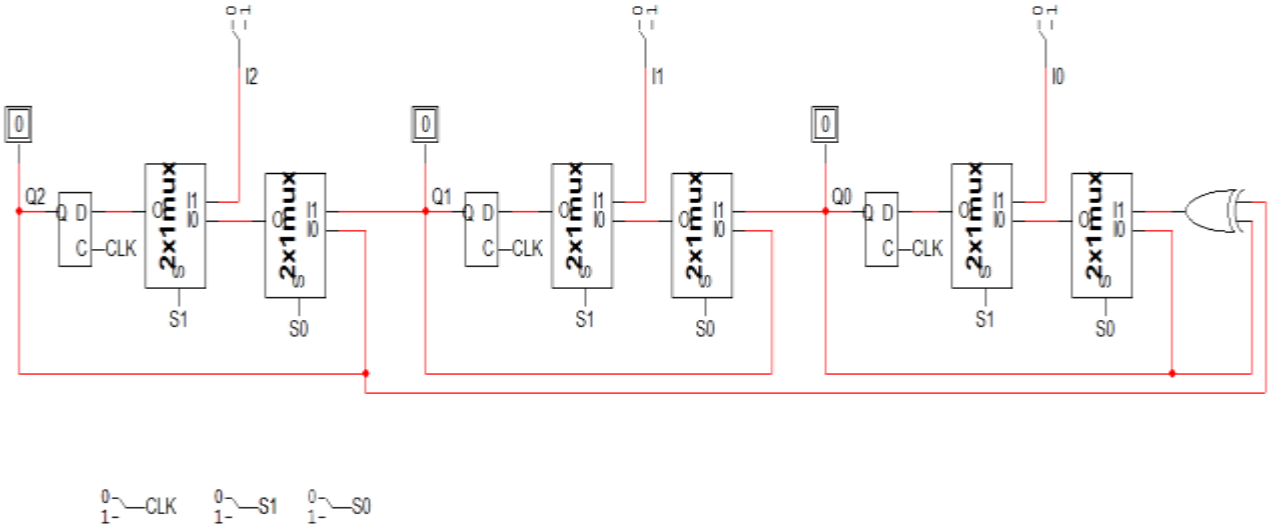
4. Complete the following timing diagram of the circuit for the inputs shown assuming that the FFs are **positive edge triggered**: (**4 points**)


Clock
Reset
X
AB
00
01
00
01
Y

Question 6: **(8 Points)**

(i) Using minimum number of D-FFs and other needed standard components and logic gates, show the design of a 3-bit register Q that has two control inputs: S1 and S0. The register has a 3-bit external input $I_2I_1I_0$. The table below shows the functionality of the register. **(4 points)**

S1	S0	Action
0	0	No change in Q
1	X	Load parallel input (i.e. $Q_2Q_1Q_0 \leftarrow I_2I_1I_0$)
0	1	$Q_2 \leftarrow Q_1$, $Q_1 \leftarrow Q_0$, $Q_0 \leftarrow Q2 \oplus Q0$



(i) Complete the following table by showing the content of register Q after each clock cycle:

(4 points)

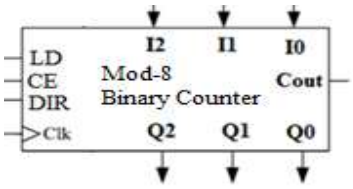
Inputs in a cycle affect the register in the next cycle

Clock #	S1	S0	I_2 I_1 I_0	Q_2 Q_1 Q_0
1	1	0	1 1 1	0 0 0
2	0	1	1 0 1	1 1 1
3	0	1	1 1 1	1 1 0
4	0	1	0 1 1	**1 0 1**
5	0	0	1 0 1	**0 1 0**
6	1	0	1 1 0	**0 1 0**
7	0	0	1 1 1	**1 1 0**

Question 7 **(13 Points)**

I) It is required to design a **mod 8 up/down counter** that has the following control inputs:

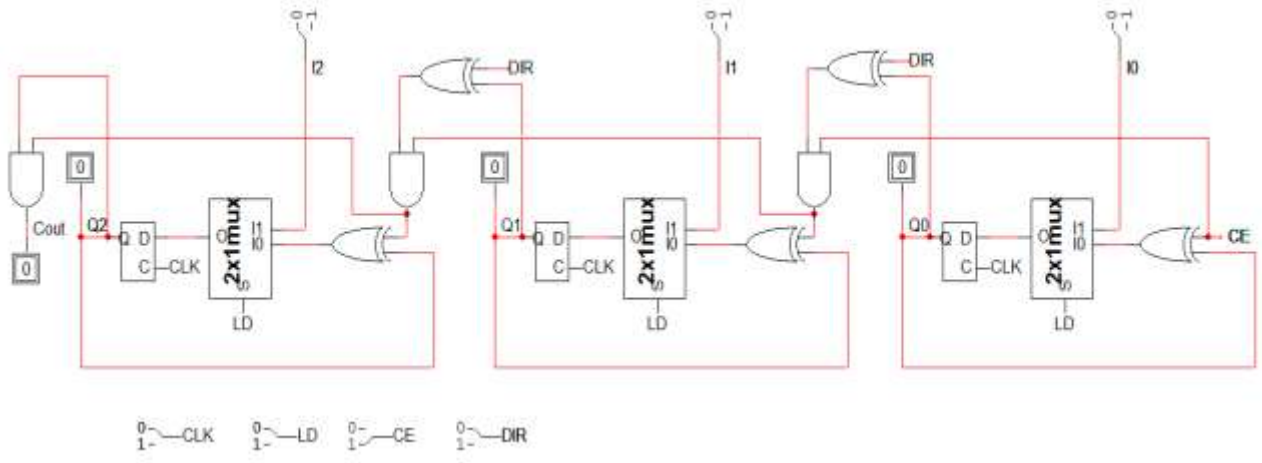
- **LD** (parallel load), together with its associated inputs I_2, I_1, I_0.
- **CE** (Count Enable)
- **DIR (**when 0 counting up and when 1 counting down**)**



The counter produces an output signal (**C_{out}**) which equals **1** when its output equals 7 when DIR=0 and CE=1 OR when its output equals 0 when DIR=1 and CE=1. Design the counter using D-FFs and **minimum** number of **logic gates and minimum-size Multiplexers**. **Note: Do not use an adder in your solution.**

(6 Points)

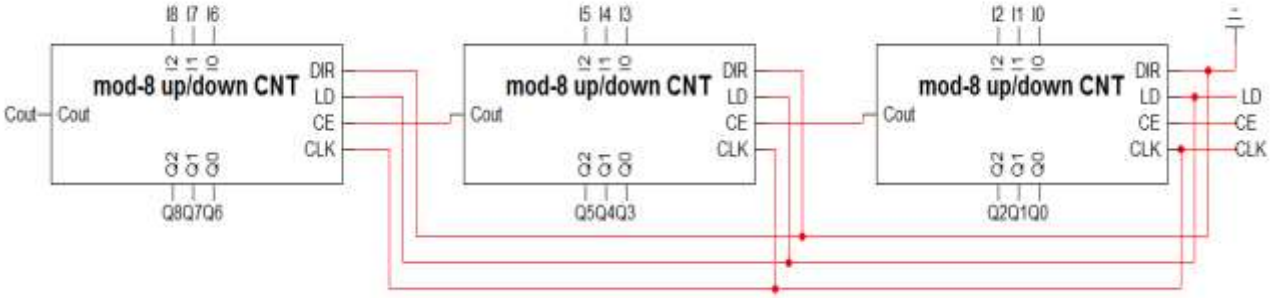
LD	CE	DIR	**Counter Next Content after the clock pulse** $(Q_2Q_1Q_0)^+$
1	X	X	I2 I1 I0 (load)
0	1	0	$(Q_2Q_1Q_0)+1$ (Increment up by 1)
0	1	1	$(Q_2Q_1Q_0)-1$ (Decrement up by 1)
0	0	X	$Q_2Q_1Q_0$ (no change)



II) Given that the clock frequency of the **mod-8 up/down counter** is 32 MHZ, what is the clock frequency of the Q2 output of the counter when the counter is set as an up counter? **(1 Point)**

The clock frequency of Q2 will be 32 MHZ / 8 = 4 MHZ.

III) Using any number of the above **mod 8 up/down counter** and other needed logic gates design a **mod 512 up counter**, which has the control inputs: LD, and CE. Clearly label all inputs and outputs. Note that only an **up counter** is required. **(3 Points)**



IV) Modify your design in (III) to obtain a clock frequency divider that divides the clock frequency by **258**. Show the signal to be used as a clock that has the divided frequency with the name CLK_{new}.

(3 Points)