***King Fahd University of Petroleum and Minerals***

***College of Computer Science and Engineering***

***Computer Engineering Department***

**COE 202: Digital Logic Design (3-0-3)**

**Term 132 (Spring 2013)**

**Final Exam**

**Monday May 19, 2014**

**8:00 a.m. – 10:30 a.m.**

**Time: 150 minutes, Total Pages:**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_**

**Notes:**

* Do not open the exam book until instructed
* Calculators are not allowed (basic, advanced, cell phones, etc.)
* Answer all questions
* All steps must be shown
* Any assumptions made must be clearly stated

|  |  |  |
| --- | --- | --- |
| **Question** | **Maximum Points** | **Your Points** |
| **1** | **10** |  |
| **2** | **10** |  |
| **3** | **11** |  |
| **4** | **18** |  |
| **5** | **15** |  |
| **6** | **6** |  |
| **Total** | **70** |  |

**Question 1. (10 Points)**

Answer the following questions by **filling** the spaces with the correct answers:

1. Given a synchronous sequential circuit with 17 states, the minimum number of flip-flops required to implement the circuit is \_\_\_\_\_\_ flip flops and the number of unused states is \_\_\_\_\_\_\_\_\_ states. **(2 points)**
2. For a 3-bit synchronous binary counter (outputs Q2, Q1 and Q0), with input clock frequency of 32 MHZ, the frequency of Q0 is \_\_\_\_\_\_ MHZ and the frequency of Q2 is \_\_\_\_\_\_ MHZ. **(2 points)**



1. For the circuit shown rights, sketch the output waveforms at Q and y given the shown input waveforms of the clock signal *clk* and the input signal *x*. **(6 Points)**

(*Note: Neglect propagation delays*)

C



Question 2. (**10 points)**

The sequential circuit shown below has a single output Z, an input *x* together with a Reset input to initialize the circuit. Note that the used D-FFs have direct/asynchronous Clear and Set inputs (shown in the figure as CLR and SET).



1. Is the circuit type Mealy or Moore? Why? ( 2 point)

Mealy since Z depends on the input *x*.

1. Derive expressions for the D0 and D1 flip flop inputs and the external output Z. (3 points)

$$D\_{0}=y\_{1}y\_{0}+\overbar{x} \overbar{y\_{0}}$$

$$D\_{1}=y\_{0}⊕x$$

$$Z=y\_{1}+D\_{1}$$

1. Derive the state transition table of the circuit. (4 points)

|  |  |  |
| --- | --- | --- |
| **PS** | **NS (y1+ y0+)** | **Z** |
| (y1 y0) | *x* = 0  *x* = 1 | *x* = 0  *x* = 1 |
|  0 0 |  0 1 1 0 |  1 0 |
|  0 1 |  1 0 0 0 |  0 0 |
|  1 1 |  1 1 0 1 |  1 1 |
|  1 0 |  0 1 1 0 |  1 1 |

1. What is the circuit initial state? (1 points)

$$y\_{1}y\_{0}=10$$

**Question 3. (11 Points)**

A **Moore**  *odd parity checker* circuit has a single input *x* and a single output signal *error.* The input consists of 4-bit chunks (3-data bits + a fourth parity bit) that are *serially received* at the input *x.* The *error* output is 1 whenever the received 4-bit stream has even number of 1’s, and 0 otherwise. Draw the state diagram of this circuit.

(**NOTE**: You are *only* required to draw the state diagram **Nothing MORE**)

time

t = 0

Example:

|  |  |  |
| --- | --- | --- |
| Input | ***x*** |  0 1 0 1\_1 1 1 0\_1 0 1 1\_1 1 1 1  |
| Output | ***error*** |  0 0 0 0\_**1** 0 0 0\_**0** 0 0 0\_**0** 0 0 0\_**1** |

**Question 4. (18 Points)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Current State** | **X** | **Y** | **Next State** | **Z** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

1. Given the following state table of a synchronous sequential circuit which has two inputs (X ,Y) and one output (Z); is this circuit a Moore or Mealy design? (1 points)

Mealy

1. Consider a 4-bit counter with the following control inputs:
* Synchronous load (LD) that loads the inputs (I3I2I1I0) when high (LD=1).
* Synchronous clear (CLR) that clears the counter when low (CLR=0).
* Enable input (E) that enables the counter when high (E=1).
	1. Add necessary gates to convert this counter to a decade counter, i.e. modulo 10 counter (3 points)



* 1. Add necessary gates to give the above decade counter cascading capability and then connect these decade counters together to build a three decimal digits counter to count from 000 to 999. (4 points)





1. Design a 4-bit counter using a 4-bit register with any needed logic gates/MSI components. The counter should have three synchronous control inputs. These inputs work as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **CLR** | **LD** | $$up/\overbar{dwn})$$ | **Action with next effective edge** |
| 0 | X | X | Clear  |
| 1 | 1 | X | Parallel Load  |
| 1 | 0 | 0 | Decrement *by one* |
| 1 | 0 | 1 | Increment *by three* |

 (10 points)

