King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)

Term 132 (Spring 2013)

Final Exam

Monday May 19, 2014

8:00 a.m. – 10:30 a.m.

Time: 150 minutes, Total Pages: 9

Name: _____ ID: _____ Section: _____

Notes:

- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	10	
2	10	
3	11	
4	18	
5	15	
6	6	
Total	70	

Question 1. **(10 Points)**

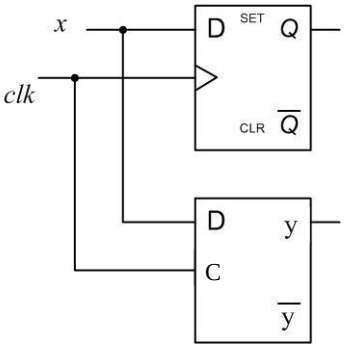
Answer the following questions by **filling** the spaces with the correct answers:

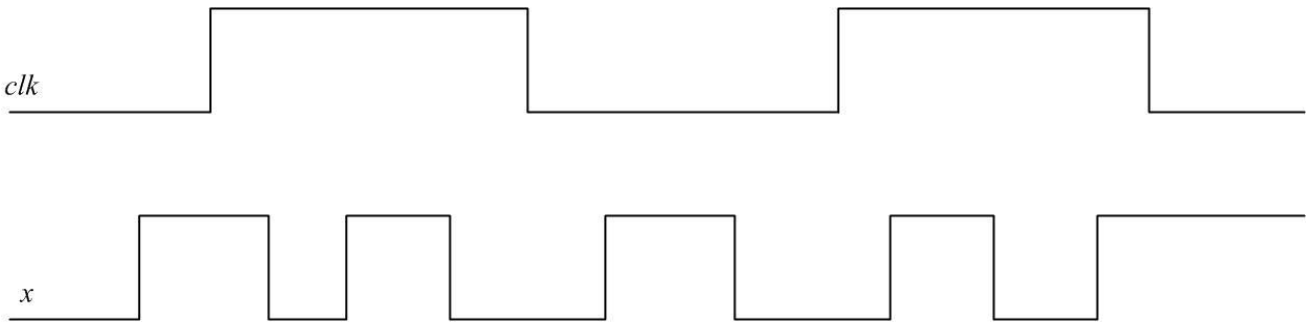
i. Given a synchronous sequential circuit with 17 states, the minimum number of flip-flops required to implement the circuit is _____ flip flops and the number of unused states is _____ states. **(2 points)**

ii. For a 3-bit synchronous binary counter (outputs Q_2, Q_1 and Q_0), with input clock frequency of 32 MHZ, the frequency of Q_0 is _____ MHZ and the frequency of Q_2 is _____ MHZ. **(2 points)**

iii. For the circuit shown rights, sketch the output waveforms at Q and y given the shown input waveforms of the clock signal *clk* and the input signal *x*. **(6 Points)**

(*Note: Neglect propagation delays*)



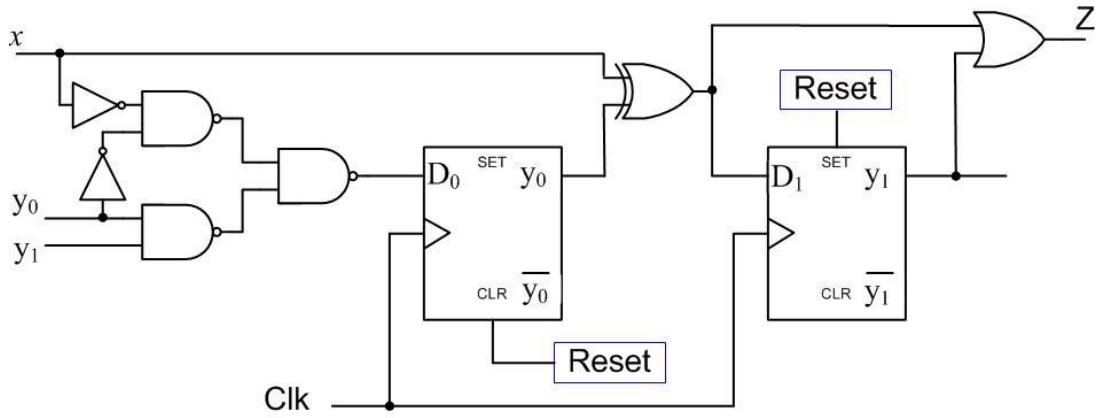


Q

y

Question 2. **(10 points)**

The sequential circuit shown below has a single output Z, an input *x* together with a Reset input to initialize the circuit. Note that the used D-FFs have direct/asynchronous Clear and Set inputs (shown in the figure as CLR and SET).



a. Is the circuit type Mealy or Moore? Why? (2 point)

b. Derive expressions for the D_0 and D_1 flip flop inputs and the external output Z. (3 points)

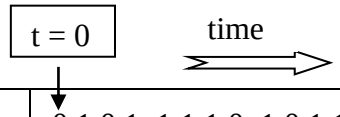
c. Derive the state transition table of the circuit. (4 points)

d. What is the circuit initial state? (1 points)

Question 3. **(11 Points)**

A **Moore** *odd parity checker* circuit has a single input *x* and a single output signal *error.* The input consists of 4-bit chunks (3-data bits + a fourth parity bit) that are *serially received* at the input *x.* The *error* output is 1 whenever the received 4-bit stream has even number of 1's, and 0 otherwise. Draw the state diagram of this circuit.
(**NOTE**: You are *only* required to draw the state diagram **Nothing MORE**)

Example:



Input	***x***	0 1 0 1_1 1 1 0_1 0 1 1_1 1 1 1
Output	***error***	0 0 0 0_**1** 0 0 0_**0** 0 0 0_**0** 0 0 0_**1**

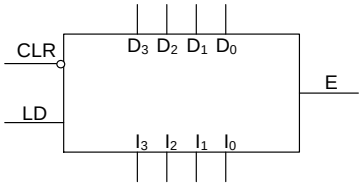
Question 4. **(18 Points)**

I. Given the following state table of a synchronous sequential circuit which has two inputs (X ,Y) and one output (Z); is this circuit a Moore or Mealy design? (1 points)

Current State	X	Y	Next State	Z
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

II. Consider a 4-bit counter with the following control inputs:

- Synchronous load (LD) that loads the inputs ($I_3I_2I_1I_0$) when high (LD=1).
- Synchronous clear (CLR) that clears the counter when low (CLR=0).
- Enable input (E) that enables the counter when high (E=1).



a. Add necessary gates to convert this counter to a decade counter, i.e. modulo 10 counter (3 points)

b. Add necessary gates to give the above decade counter cascading capability and then connect these decade counters together to build a three decimal digits counter to count from 000 to 999. (4 points)

III. Design a 4-bit counter using a 4-bit register with any needed logic gates/MSI components. The counter should have three synchronous control inputs. These inputs work as follows:

CLR	**LD**	**up/$\overline{\text{dwn}}$)**	**Action with next effective edge**
0	X	X	Clear
1	1	X	Parallel Load
1	0	0	Decrement *by one*
1	0	1	Increment *by three*

(10 points)

Question 5. **(15 Points)**

Consider the following state transition table for a synchronous sequential circuit that multiplies a binary number by 3 i.e. Z=3*X. The circuit has a single input **X**, a single output **Z**, and two state variables $\mathbf{Y_0}$, and $\mathbf{Y_1}$. The states are encoded using binary codes **00**, **01**, **10.**

PS $(\mathbf{Y_1}\ \mathbf{Y_0})^t$	**NS** $(\mathbf{Y1}\ \mathbf{Y_0})^{t+1}$		**Z**	
	X = 0	**X = 1**	**X = 0**	**X = 1**
0 0	0 0	0 1	0	1
0 1	0 0	1 0	1	0
1 0	0 1	1 0	0	1

(i) Using D-FFs and **<u>minimal</u>** combinational logic, determine the equations for the D-FF inputs and the output Z for this circuit and draw the resulting circuit. (6 points)

(ii) You are required to implement the above circuit using a **ROM** and a **register**.

a. What is the minimum size of the ROM (number of memory locations × number of memory bits per location)? (2 points)

b. Draw the block diagram for such implementation. (**Label all components inputs and outputs together with various signals**) (3 points)

c. Starting at the initial state **00**, what is the sequence of ROM location addresses that will be accessed when applying the input sequence **X = 1100** where **1** is applied first. (2 points)

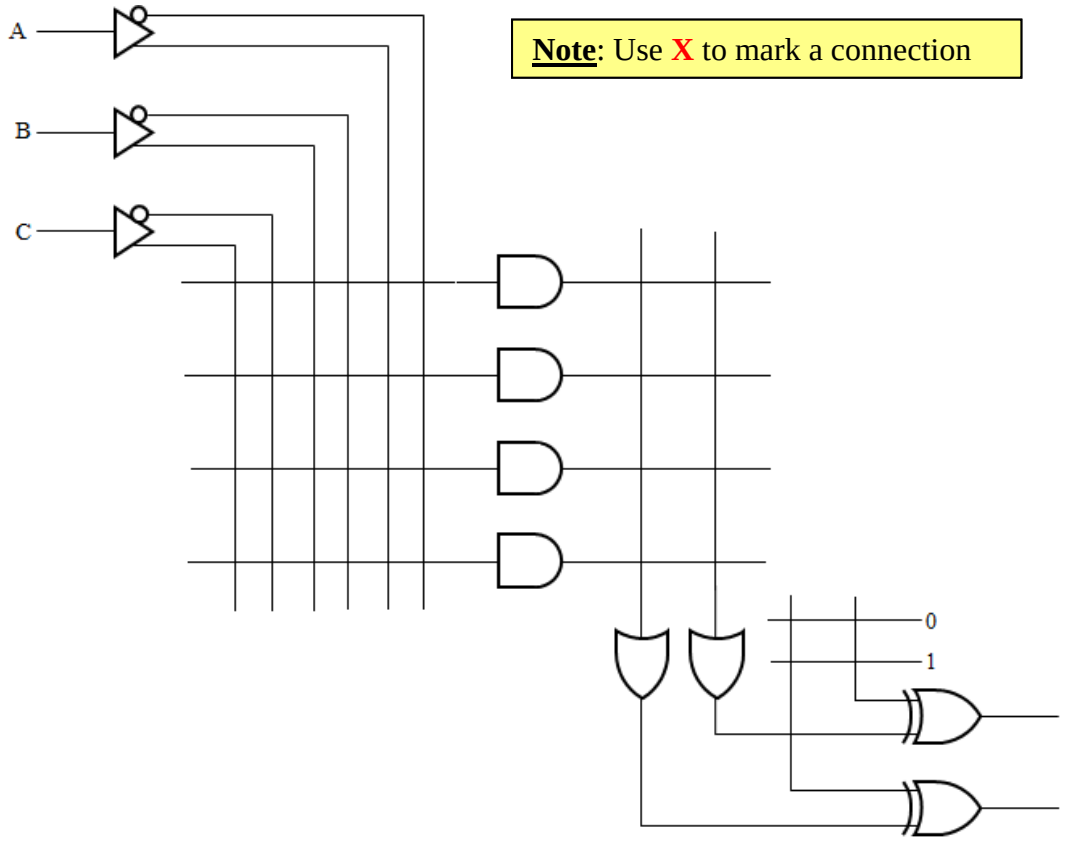
d. Starting from address **0,** fill in the following table to show the data stored in the first four memory locations in the ROM device (2 points)

Binary Address	**Binary Stored Data**

Question 6. **(6 Points)**

The two functions F_1 and F_2 are to be implemented using the PLA shown below. Indicate the links to be programmed/connections in the PLA such that the *number of product terms is minimized*.

$F_1(A, B, C)=\Sigma\, m(0, 1, 2, 4, 6)$
$F_2(A, B, C)=\Sigma\, m(0, 1, 3, 5, 7)$



Note: Use **X** to mark a connection