King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

COE 202: Digital Logic Design (3-0-3)
Term 101 (Fall 2010)
Final Exam
Monday, January 24th, 2011

Time: 7 pm

Name:_____ ID:_____ Section: _____

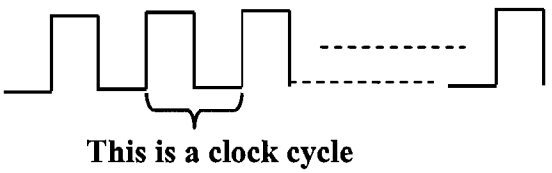
Notes:

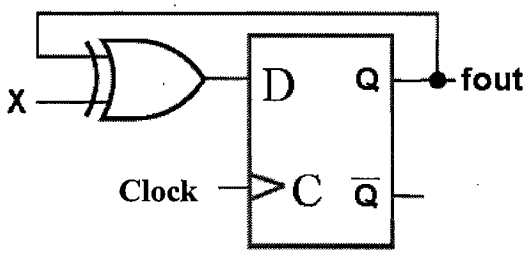
- Do not open the exam book until instructed
- Calculators are not allowed (basic, advanced, cell phones, etc.)
- Answer all questions
- All steps must be shown
- Any assumptions made must be clearly stated

Question	Maximum Points	Your Points
1	15	
2	10	
3	10	
4	15	
5	20	
6	10	
7	15	
8	10	
Total	105	

Q1) **(15 marks)**

a. The clock of the D flip flop is a 10 Hz square signal (i.e. 10 cycles or pulses/seconds). Fill in the table below for the frequency of the signal at the Q output: **(4 points)**



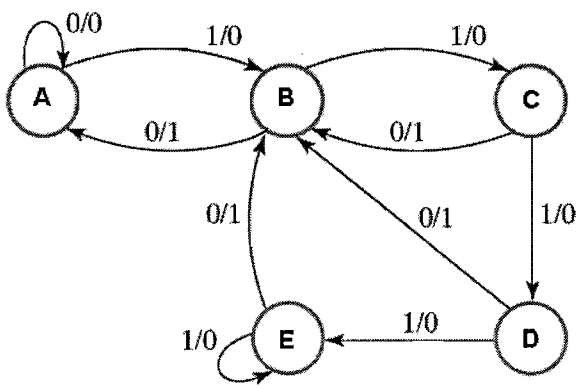


Control input (X)	Frequency fout (Hz or pulses/seconds)
0	0
1	5

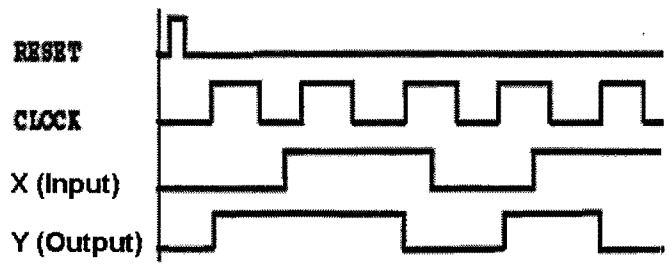
b. For a regular 4-bit synchronous Up Binary counter that is always enabled (assuming that it is initially at zero i.e. the outputs are 0000), the counter outputs will become 0111 after 7 clock cycles. After 10 more clock cycles, the counter outputs will be 0001. **(2 points)**

c. The state diagram below represents the behavior of a Mealy/Moore sequential circuit with a minimum of 3 (how many) flip flops and 1 (how many) inputs.

When the circuit is in state C, a minimum of 2 (how many) clock pulses will be required to return it to state C again. **(4 points)**



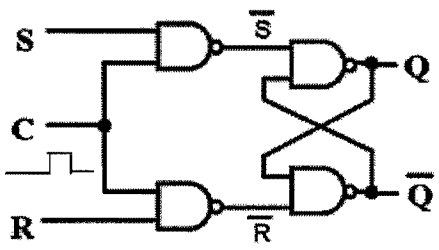
d. The timing diagram below partially represents waveforms of a _____(Mealy/Moore) sequential circuit with an external input X and an external output Y. The flip flops change their outputs on the _____ (positive/negative) edge of the clock. **(2 points)**



e. For the clocked S-R latch using NAND gates shown below, complete the waveform of the Q output for the given S, R, and clock (C) inputs. Initially, the Q output is at 0 logic. Ignore any propagation delays. **(3 points)**

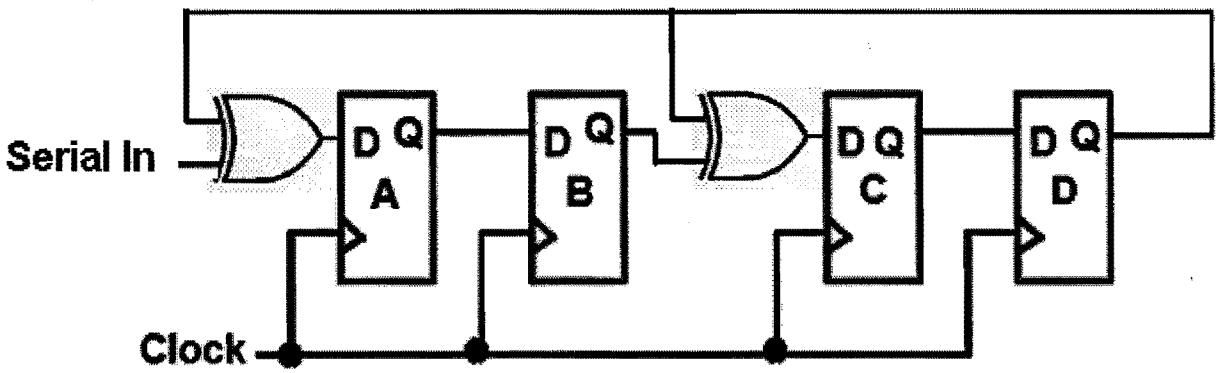
S	1	1	0	0	0	1	1
R	0	1	1	0	0	1	1
C	0	0	0	1	0	0	1
Q	0	0	0	0	0	0	{1
Q'	1	1	1	1	1	1	{1

or undefined



Q2) **(10 points)**

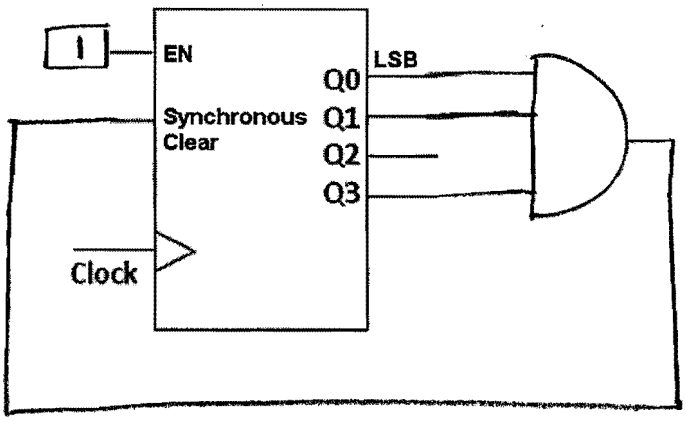
Refer to the special shift register circuit shown below. The circuit has 4 stages of D flip flops and a serial input. Initially the register has the contents ABCD = 0110. For the sequence of the serial input shown in the table below, fill in the spaces in the table to indicate the register contents following the arrival of each of the next five clock pulses. In the last column, express the contents in hex (Stage D is the LSB).



Clock Pulse #	Serial Input, just **before** the arrival of the next clock pulse	A	B	C	D	Register Contents in Hex
Initial State	1	0	1	1	0	6
1	0	1	0	1	1	B
2	1	1	1	1	1	F
3	1	0	1	0	1	5
4	0	0	0	0	0	0
5	1	0	0	0	0	0

Q3) **(10 points)**

You are given the 4-bit binary synchronous up counter shown below. The counter has an Enable input (EN) and a synchronous CLEAR input.



a. Add to the counter the minimum necessary logic required to implement a modulo-12 counter. Indicate all necessary inputs to the counter. **(5 points)**

b. The counter developed has a counting cycle that starts with count 0 (in decimal) and ends with count 11 (in decimal) **(2 points)**

c. With a clock frequency of 60 Hz (or 60 cycles/second), the frequency of the signal at output Q3 would be 5 Hz. **(1 point)**

60/12 = 5

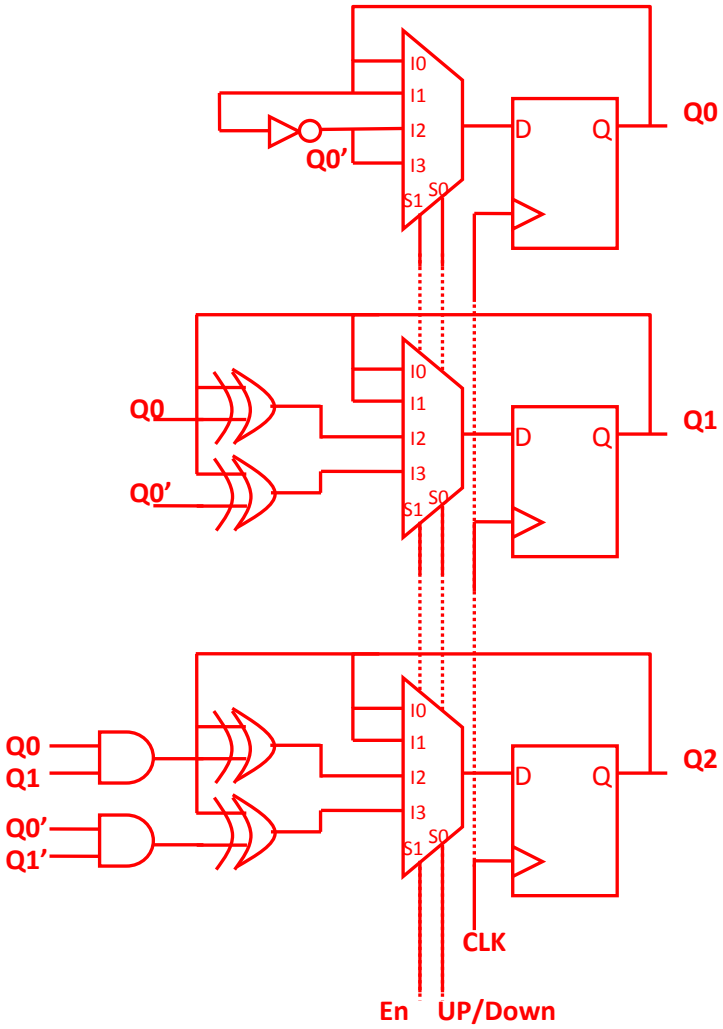
d. Would the circuit work properly if the Clear input was a direct (asynchronous) input? Justify your answer briefly. **(2 points)**

No.
The direct 'clear' will change the counter outputs at once which, in turn, will make the 'clear' condition disappear

Q4) **(15 points)**

a. Using D-FFs and any other components of your choice, design a **3-bit counter** with two control signals (inputs); Enable and UP/DOWN. When Enable = 0, the counter's output stays the same. When Enable = 1, then if the UP/DOWN input = 1, then the counter counts up (0 → 1 → 2 → 3 …) and if UP/DOWN input = 0 then the counter counts down (7 → 6 → 5 → … → 0 → 7).

(10 points)



b. Assuming that the counter starts from zero (all FFs are reset to zero), specify the counter output for the following sequence of inputs: **(5 points)**

En		**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**
UP/DOWN		**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**
Counter Output	**MSB**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
		0	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
	LSB	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**

Q5) **(20 Points)**

Design a circuit that detects the occurrence of **three consecutive 1s** (i.e. 111) in an input stream (X) and produces an output pulse for one clock cycle (i.e. the output will be 1 for one clock cycle). The circuit **will not consider overlapping sequences as different sequences.** e.g. 11110 is only one sequence followed by 10, so the output Y, will be 1 for only one cycle in this case. 111111 are two consecutive cycles, but Y will look like this 001001.

Use minimum number of D-FFs and gates to implement the circuit (use AND, OR and NOT gates only).

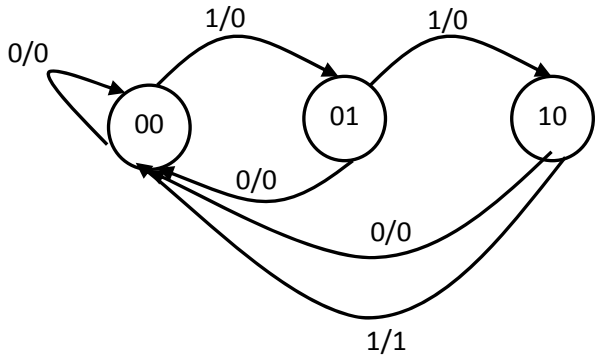
Mealy Implementation

Two D-FFs, A and B:

DA=A+=A'BX ,

DB=B+=A'B'X ,

Y=AB'X



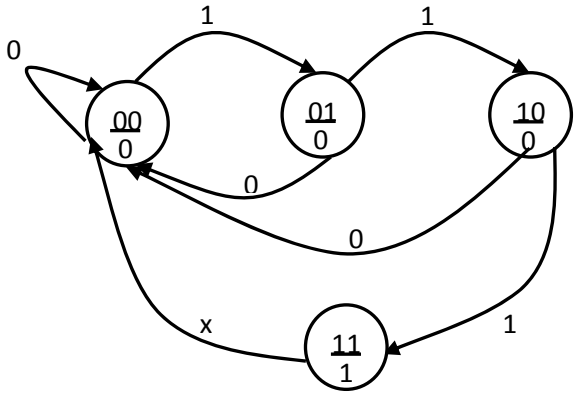
Moore Implementation

Two D-FFs, A and B:

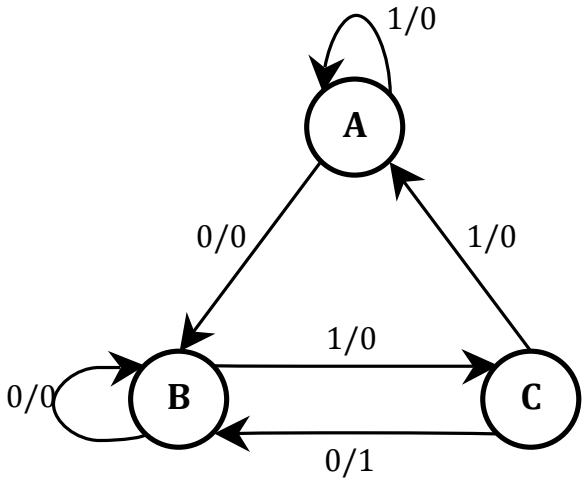
DA=A+=A'BX + AB'X ,

DB=B+=A'B'X + AB'X = B'X ,

Y=AB



Q6) **(10 points)**

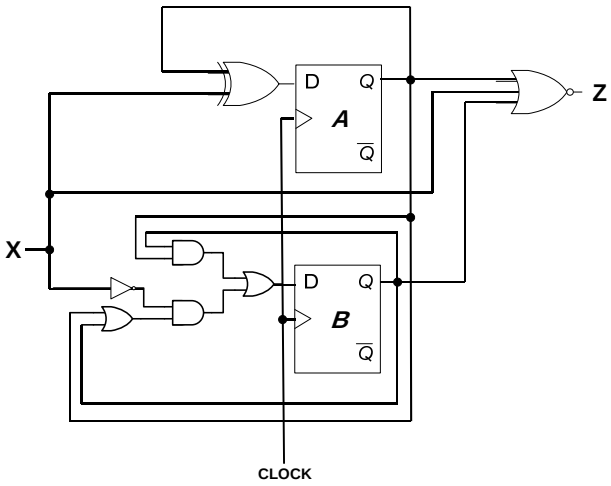


The above figure shows a state diagram of a sequential circuit with one input *x* and one output *y*. Trace the state transitions of this circuit by determining the output and the next state given the sequence of inputs and an initial state as shown in the table.

State	**A**	A	B	C	B	C	A	B	B	C
x	**1**	0	1	0	1	1	0	0	1	0
y	**0**	0	0	1	0	0	0	0	0	1

Q7) **(15 points)**

Derive the state diagram for the following circuit:



Expressions for FFs' inputs & external output:

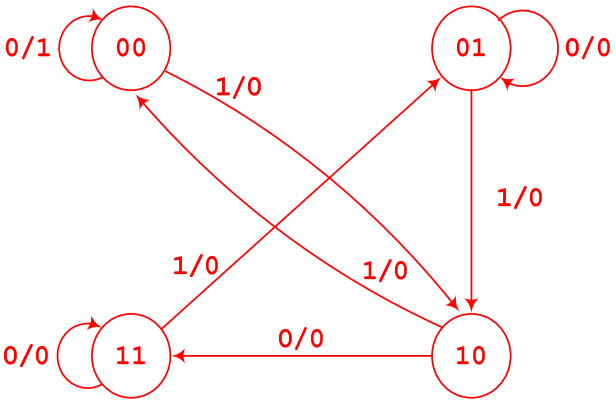
$$Q_A^+ = D_A = Q_A \oplus X$$

$$Q_B^+ = D_B = Q_A \cdot Q_B + (Q_A + Q_B) \cdot \overline{X}$$

$$= Q_A \cdot Q_B + Q_A \cdot \overline{X} + Q_B \cdot \overline{X}$$

$$Z = \overline{Q_A + Q_B + X} = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{X}$$

Q_A	Q_B	X	Q_A^+	Q_B^+	Z
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	0	1	0



Q8) **(10 points)**

Using *D* flip-flop(s) and MUX(s) **only** (i.e., other components are not allowed), draw the logic diagram for a **4-bit register** with mode selection inputs S_1S_0. The register should operate according to the following table:

S_1S_0	Register operation
00	Hold the current contents of the register (i.e. stay the same)
01	Parallel load (load inputs into register in parallel)
10	Rotate ***right*** (i.e., shift register contents to the ***right*** feeding in the shifted bit out from the last bit location as a serial input to the first location)
11	Load the register with the 1's complement of the current content.

You must clearly label the D flip-flop(s) and MUX(s) used together with all inputs and outputs.