COE 202, Term 112

Digital Logic Design

Assignment# 5

Due date: Sat. May 12

Q.1. It is required to design a 4-bit register that operates according to the following table:

S1	S0	Operation
0	0	No change
0	1	Parallel load from inputs I0, I1, I2 and I3.
1	0	Shift either left or right depending on Dir input. When Dir=0 shift left, and when Dir=1 shift right.
1	1	Count either up or down depending on Dir input. When Dir=0 count up, and when Dir=0 count down.

The register has the inputs S1, S0 and Dir to control its operation. It also has four inputs I0, I1, I2 and I3 for parallel load. Assume that the input I0 is used for serial shifting either to the left or to the right. Assume also that the register can be set asynchronously to 0 by a reset signal Reset. The register produces four outputs, Q0, Q1, Q2, and Q4. Your design should be a synchronous sequential circuit.

(i) Design the four bit register in a modular manner by designing 1-bit and replicating it four times.

(ii) Model your design in logic works.

(iii) Test your design and verify its correctness by simulation and show snapshots that demonstrate its correct functionality for all operations.

This assignment can be solved as a group of two students. Submit your solution as a word document along with the circuit in one zipped file.