COE 202, Term 132

Digital Logic Design

Assignment# 4

Due date: Tuesday May 13

Q.1.

(i) Design a 4-bit up-down synchronous counter that has an enable input, EN, that enables counting and a direction input, DIR, that makes the counter count up when DIR=0 and counts down when DIR=1, and a load input, LD, that when set to 1 loads the counter with an initial value.

(ii) Model the 4-bit up-down counter in logic works and demonstrate its correct functionality by simulation.

(iii) Design a seconds up-down counter (i.e. modulo 60 counter that counts between 0 and 59) based on the counter you designed in (i).

(iv) Model the seconds up-down counter in logic works and demonstrate its correct functionality by simulation. Load the counter with the value 55 and show its counting up until the value 2 and then change the counter to count down and show its simulation until it reaches the value 55.

Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuits in one zipped file.