COE 202, Term 122

Digital Logic Design

Assignment# 4

Due date: Sat. May 11

Q.1. It is required to design a synchronous sequential circuit that receives a serial input **X** and produces a serial output **Z**. The output Z will be 1 if the input has been **alternating for at least 3 clock periods**. An input is considered alternating if its value changes from 0 to 1 or from 1 to 0. Assume the existence of an asynchrnous reset input to reset the machine to a reset state. The following is an example of some input and output streams:

Example:

Input	**X**	1 0 1 0 1 0 1 1 0 1 0 1 0 0 1 0
Output	**Z**	0 0 0 1 1 1 1 0 0 0 1 1 1 0 0 0

(i) Derive the state diagram of the circuit assuming a **Mealy** model.

(ii) Implement your design using D flip flops with minimal number of flip flops and combinational logic.

(iii) Model your design in logic works.

(iv) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness.

Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuits in one zipped file.