COE 202, Term 121

Digital Logic Design

Assignment# 4

Due date: Mon. Dec. 24

Q.1. It is required to design a 4-bit counter that operates according to the following table:

S1	S0	Operation
0	0	No change
0	1	Parallel load from inputs I0, I1, I2 and I3.
1	0	Count Up
1	1	Count Down

The counter has the inputs S1, S0 to control its operation. It also has four inputs I0, I1, I2 and I3 for parallel load. Assume also that the register can be set asynchronously to 0 by a reset signal Reset. The register produces four outputs, Q0, Q1, Q2, and Q4. Your design should be a synchronous sequential circuit.

(i) Design the 4-bit counter in a modular manner by designing 1-bit and replicating it four times.

(ii) Model your design in logic works.

(iii) Test your design and verify its correctness by simulation and show snapshots that demonstrate its correct functionality for all operations.

Q.2. Use the 4-bir register designed in (Q1) to design a modulo-6 up/down counter i.e., a counter that counts through the sequence {0, 1, 2, 3, 4, 5}.

(i) Model your design in logic works.

(ii) Test your design and verify its correctness by simulation and show snapshots that demonstrate its correct functionality for all operations.

This assignment can be solved as a group of two students. Submit your solution as a word document along with the circuit in one zipped file.