COE 202, Term 112

Digital Logic Design

Assignment# 4

Due date: Sat. May 5

Q.1. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects either the sequence 1010 or the sequence 1110 assuming overlapping sequence detection. Design the circuit as Mealy machine. Assume the existence of a reset input to reset the machine to a reset state. Model the circuit using logic works and verify its correctness by simulation.

(i) Derive the state diagram for your circuit, and then obtain the circuit implementation optimizing the output and next state equations assuming D-FFs.

(ii) Model the circuit using logic works.

(iii) Test your design and verify its correctness by simulation by showing the output resulting from applying the following sequence X={111101010110100}. Show snapshots of your simulation to demonstrate its correctness.

This assignment can be solved as a group of two students. Submit your solution as a word document along with the circuit in one zipped file.