COE 202, Term 203

Digital Logic Design

Assignment# 4

Due date: Saturday, August 7, 2021

It is required to design a synchronous sequential circuit that receives a serial input X that produces 1 when the input sequence is either {0110} (i.e., 0 followed by 1 followed by 1 followed by 0) or {1100} (i.e., 1 followed by 1 followed by 0 followed by 0) assuming overlapping sequences. The output Z is also a bit stream that produces a 1 only after detecting any of the two sequences. Use an asynchronous reset input to reset the sequential circuit to its initial state.

Example:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Clock cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| X | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| Z | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**a)** (10 points) Draw a Mealy state diagram of the sequential circuit.

**b)** (10 points) Implement your design using a minimal number of D-type flip flops and combinational logic. Specify the K-maps and write the minimal next state and output equations.

**c)** (10 points) Write a structural Verilog model that models your implemented sequential circuit by modeling the D Flip-Flops and instantiating them and modeling the combinational part using either assign statement or gate primitives.

**d)** (10 points) Write a behavioral Verilog description that models your state diagram in part (a).

**e)** (10 points) Write a test bench that tests BOTH the structural Verilog model of part (c) and the behavioral Verilog model of part (d) using the example input sequence shown above. Call the outputs Z1 and Z2 for the models in (c) and (d), respectively. Start by resetting all flip-flops and then apply the input sequence of X. Verify that your circuit produces the correct output by including the generated waveform from simulation and comparing to the given example above.

f) Submit a report (Word or PDF document) that should contain:

1. The state diagram of your design (part a).
2. The state table, K-maps, and logic equations of your sequential circuit (part b).
3. A copy of the Verilog modules and test benches of parts (c), (d), and (e).
4. The timing diagrams (waveforms) taken directly as snapshots from the simulator for parts (e) and analysis of output.

The assignment can be solved individually, or in groups of two students. Submit a soft copy of the report on Blackboard.