COE 202, Term 142

Digital Logic Design

Assignment# 4

Due date: Tuesday, May 12

Q.1. It is required to design a synchronous sequential circuit that receives a serial input **X** and produces a serial output **Z** that is set to 1 when the circuits detects either the sequence 1010 or the sequence 1001. Assume that the detection of sequences is overlapping. Assume the existence of an asynchronous reset input to reset the machine to a reset state. The following is an example of an input/output stream:

Example:

Input	**X**	1 0 1 0 1 0 0 1 0 1 0 0 0
Output	**Z**	0 0 0 1 0 1 0 1 0 0 1 0 0

(i) Derive the state diagram of the circuit assuming a **Mealy** model.

(ii) Implement your design using D flip flops with minimal number of flip flops and combinational logic.

(iii) Write a structural Verilog model that models your implemented sequential circuit by modeling the D Flip-Flops and instantiating them and modeling the combinational part using either assign statement or gate primitives.

(iv) Write a test bench that tests your structural Verilog model in (iii) using the given input sequence. Verify that your circuit produces the correct output by including the generated waveform from simulations.

(v) Write a behavioral Verilog model that models your state diagram in (i).

(vi) Use the test bench developed in (iv) to test the correctness of your behavioral model developed in (v). Verify that your behavioral model produces the correct output by including the generated waveform from simulations.

This assignment can be solved based on a group of two students. Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the Verilog models in one zipped file.