COE 202, Term 141

Digital Logic Design

Assignment# 4

Due date: Sunday, Dec. 21

Q.1. It is required to design a synchronous sequential circuit that receives a serial input **X** and produces a serial output **Z that computes the equation Z=3*X-2**. Assume that the inserted input values of X will be such that Z will always be positive. Assume the existence of an asynchrnous reset input to reset the machine to a reset state. The following are a set of some input and output streams:

Example:

Input	**X**	1 0 1 0 0
Output	**Z**	1 0 1 1 0
Input	**X**	1 1 1 0 0
Output	**Z**	1 1 0 0 1

(i) Derive the state diagram of the circuit assuming a **Mealy** model.

(ii) Implement your design using D flip flops with minimal number of flip flops and combinational logic.

(iii) Model your design in logic works.

(iv) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness

This assignment can be solved based on a group of two students. Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuit in one zipped file.