**COE 202, Term 131**

**Digital Logic Design**

**Assignment# 3 Solution**

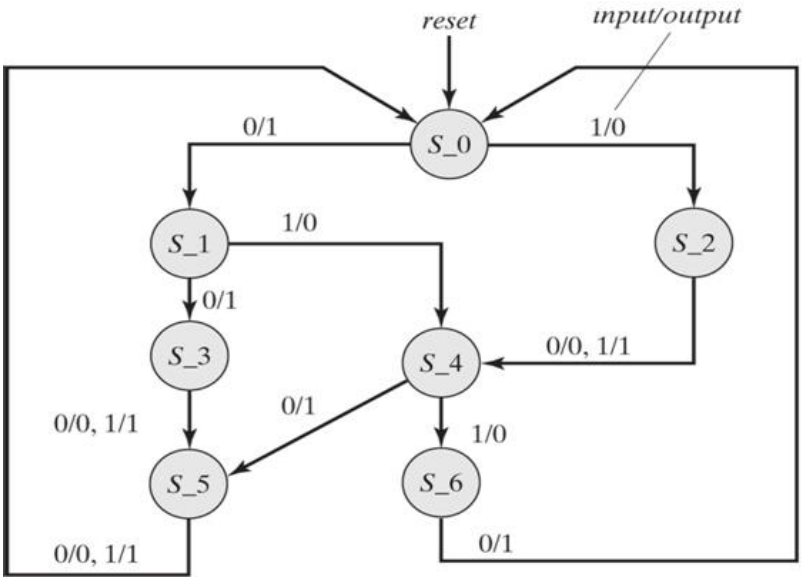
**Due date: Thursday Dec. 19**

**Q.1.** It is required to design a synchronous sequential circuit that receives BCD digits serially through input $\mathbf{B_{in}}$ and converts them to excess-3 digits and produces the result serially through output $\mathbf{B_{out}}$. Assume the existence of an asynchronous reset input to reset the machine to a reset state. The following is an example of some input and output streams:

Example:

| | | |
|---|---|---|
| Input | $\mathbf{B_{in}}$ | 0 0 0 0 1 0 1 0 1 0 0 1 1 1 1 0 |
| Output | $\mathbf{B_{out}}$ | 1 1 0 0 0 0 0 1 0 0 1 1 0 1 0 1 |

**(i)** Derive the state diagram of the circuit assuming a **Mealy** model.




**(ii)** Implement your design using D flip flops with minimal number of flip flops and combinational logic.

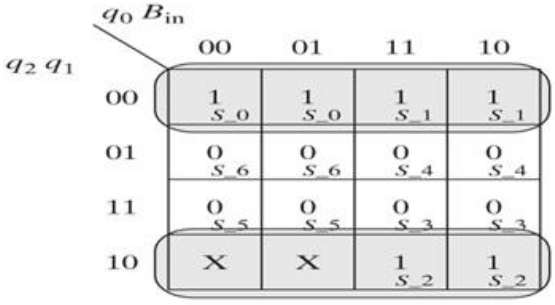
## State Table:

| Next state/output table | | |
|---|---|---|
| State | Next state/output | |
| | Input | |
| | 0 | 1 |
| $S\_0$ | $S\_1/1$ | $S\_2/0$ |
| $S\_1$ | $S\_3/1$ | $S\_4/0$ |
| $S\_2$ | $S\_4/0$ | $S\_4/1$ |
| $S\_3$ | $S\_5/0$ | $S\_5/1$ |
| $S\_4$ | $S\_5/1$ | $S\_6/0$ |
| $S\_5$ | $S\_0/0$ | $S\_0/1$ |
| $S\_6$ | $S\_0/1$ | - / - |

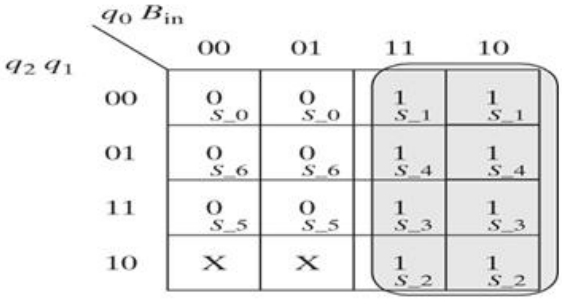
## State Encoding & State Transition Table:

| State assigment | |
|---|---|
| $q_2\,q_1\,q_0$ | State |
| 000 | $S\_0$ |
| 001 | $S\_1$ |
| 010 | $S\_6$ |
| 011 | $S\_4$ |
| 100 | |
| 101 | $S\_2$ |
| 110 | $S\_5$ |
| 111 | $S\_3$ |

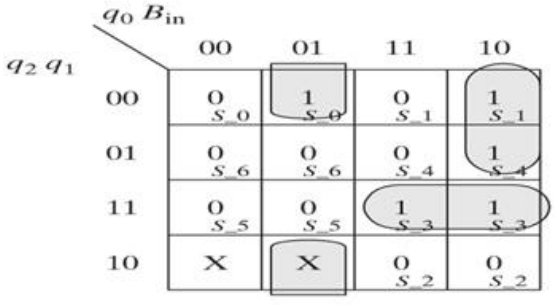
| Encoded next state/output table | | | | | |
|---|---|---|---|---|---|
| | State | Next state | | Output | |
| | $q_2\,q_1\,q_0$ | $q_2^+\,q_1^+\,q_0^+$ | | | |
| | | Input | | Input | |
| | | 0 | 1 | 0 | 1 |
| $S\_0$ | 000 | 001 | 101 | 1 | 0 |
| $S\_1$ | 001 | 111 | 011 | 1 | 0 |
| $S\_2$ | 101 | 011 | 011 | 0 | 1 |
| $S\_3$ | 111 | 110 | 110 | 0 | 1 |
| $S\_4$ | 011 | 110 | 010 | 1 | 0 |
| $S\_5$ | 110 | 000 | 000 | 0 | 1 |
| $S\_6$ | 010 | 000 | — | 1 | — |
| | 100 | — | — | — | — |



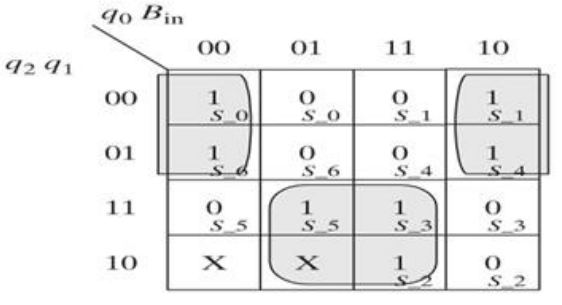

$q_0^+ = q_1'$



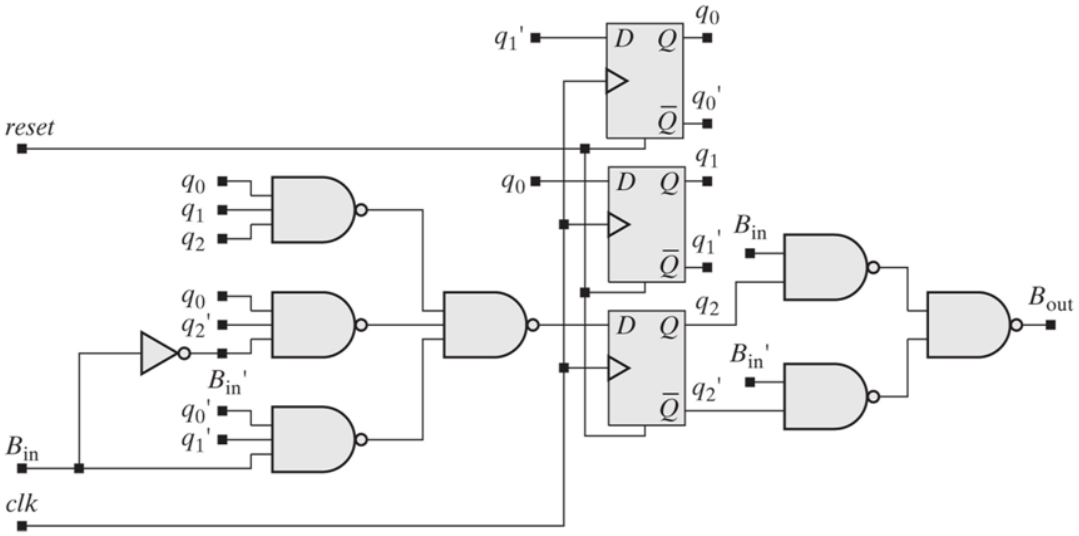

$q_1^+ = q_0$



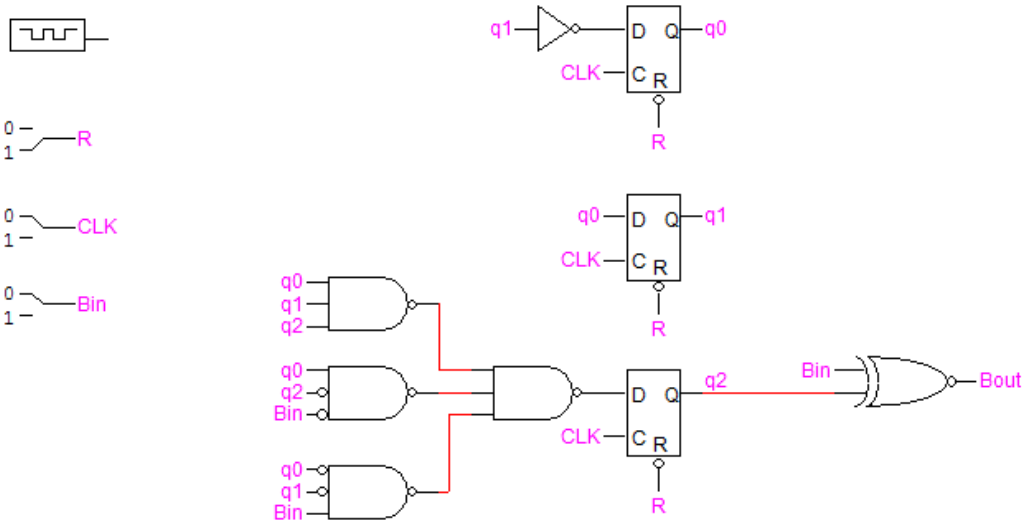

$q_2^+ = q_1'q_0'B_{in} + q_2'q_0B_{in}' + q_2\,q_1\,q_0$




$B_{out} = q_2'B_{in}' + q_2B_{in}$

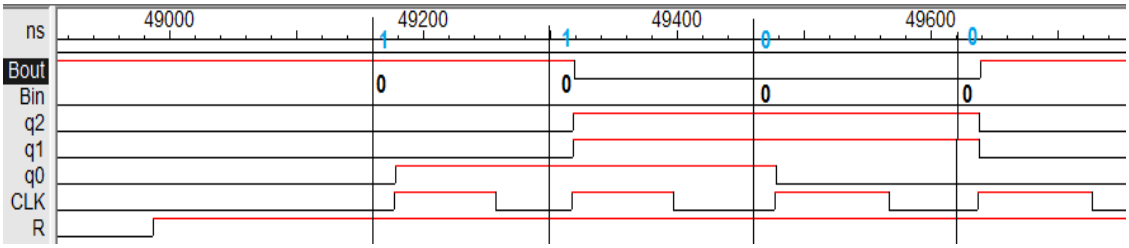


**(iii)** Model your design in logic works.




**(iv)** Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness.

When we will apply the input 0000 (i.e. decimal 0) we get the output 1100 (i.e., decimal 3) as shown in the simulation below:




When we will apply the input 1110 (i.e. decimal 7) we get the output 0101 (i.e., decimal 10) as shown in the simulation below: