

COE 202, Term 132

Digital Logic Design

Assignment# 3

Due date: Thursday May 8

Q.1. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects either the sequence 1001 or the sequence 0011 assuming overlapping sequence detection. Design the circuit as Mealy machine. Assume the existence of a reset input to reset the machine to a reset state. Model the circuit using logic works and verify its correctness by simulation.

- (i) Derive the state diagram for your circuit, and then obtain the circuit implementation optimizing the output and next state equations assuming D-FFs.
- (ii) Model the circuit using logic works.
- (iii) Test your design and verify its correctness by simulation by showing the output resulting from applying the following sequence $X=\{00100110011001\}$. Show snapshots of your simulation to demonstrate its correctness.

Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuits in one zipped file.