COE 202, Term 131

Digital Logic Design

Assignment# 3

Due date: Thursday Dec. 19

Q.1. It is required to design a synchronous sequential circuit that receives BCD digits serially through input B_{in} and converts them to excess-3 digits and produces the result serially through output B_{out}. Assume the existence of an asynchronous reset input to reset the machine to a reset state. The following is an example of some input and output streams:

Example:

Input	B_{in}	0 0 0 0 1 0 1 0 1 0 0 1 1 1 1 0
Output	B_{out}	1 1 0 0 0 0 0 1 0 0 1 1 0 1 0 1

(i) Derive the <u>state diagram</u> of the circuit assuming a **<u>Mealy</u>** model.

(ii) Implement your design using D flip flops with minimal number of flip flops and combinational logic.

(iii) Model your design in logic works.

(iv) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness.

Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuits in one zipped file.