

COE 202, Term 151

Digital Logic Design

Assignment# 3

Due date: Wednesday, Nov. 18

- Q.1.** It is required to design a circuit that receives two **4-bit** signed numbers in 2's complement representation $A=A_3A_2A_1A_0$, $B=B_3B_2B_1B_0$ and produces **5-bit output** $C= C_4C_3C_2C_1C_0$. The circuit implements the following functions based on the values of the three selection inputs: S_2 , S_1 and S_0 .

$S_2 S_1 S_0$	Function
0 0 0	$C = A + B$
0 0 1	$C = A - B$
0 1 0	$C = A + 1$
0 1 1	$C = A + 2$
1 0 0	$C = A - 1$
1 0 1	$C = A - 2$
1 1 0	$C = 2A$
1 1 1	$C = 2B$

- (i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed. Use only one adder in your solution.
- (ii) Model your design in Verilog by modeling each component separately i.e. adder, MUX, etc. and then instantiating these components to model your circuit.
- (iii) Write a Verilog test bench to test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality.

This assignment can be solved based on a group of two students. Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuit in one zipped file.