COE 202, Term 162

Digital Logic Design

Assignment# 2 Solution

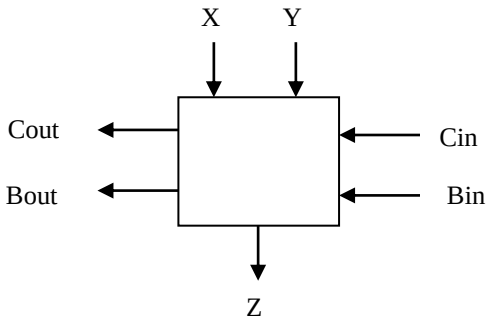
Due date: Sunday, April 9

Q.1. It is required to design an iterative combinational circuit that computes the equation Z=2*X-Y, where X and Y are n-bit unsigned numbers.

(i) Determine the number of inputs and outputs needed for your 1-bit cell.

This circuit requires the following 3 pieces of information, which can be encoded using 2 signals:

- No carry or borrow (C=0, B=0)
- Carry = 1 (C=1, B=0)
- Borrow = 1 (C=0, B=1)



(ii) Derive the truth table of your 1-bit cell.

Bin	Cin	X	Y	Bout	Cout	Z
0	0	0	0	0	0	0
0	0	0	1	1	0	1
0	0	1	0	0	1	0
0	0	1	1	0	0	1
0	1	0	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	0	1	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	0	0
1	1	0	0	X	X	X
1	1	0	1	X	X	X
1	1	1	0	X	X	X
1	1	1	1	X	X	X

(iii) Derive minimized equations for your 1-bit using K-Map method.

	00	01	11	10
00	0 0	1 1	1 3	0 2
01	1 4	0 5	0 7	1 6
11	?12	?13	?15	?14
10	1 8	0 9	011	110

Z = Bin' Cin' Y + Cin Y' + Bin Y' = Bin' Cin' Y + Y' (Cin + Bin) = Y ⊕ (Cin + Bin)

	00	01	11	10
00	0 0	0 1	0 3	1 2
01	0 4	0 5	1 7	1 6
11	?12	?13	?15	?14
10	0 8	0 9	011	010

Cout = Cin X + Bin' X Y'

	00	01	11	10
00	0 0	1 1	0 3	0 2
01	0 4	0 5	0 7	0 6
11	?12	?13	?15	?14
10	1 8	1 9	011	010

Bout = Bin X' + Cin' X' Y

(iv) Write a Verilog model for modeling your 1-bit cell by using an assign statement for each output.

```
module Cell2XMY (output Bout, Cout, Z, input Bin, Cin, X, Y);

    assign Z = Y ^  (Cin | Bin);
    assign Cout = Cin & X |  ~Bin & X & ~Y;
```

```
    assign Bout =  Bin & ~X | ~Cin & ~X & Y;

endmodule
```

(v) Write a Verilog model for modeling a 4-bit circuit based on the 1-bit model you have.

```
module D2XMY (output Bout, Cout, output [3:0] Z, input [3:0] X, Y);

wire  [2:0] C, B;

Cell2XMY M1 (B[0], C[0], Z[0], 1'b0, 1'b0, X[0], Y[0]);
Cell2XMY M2 (B[1], C[1], Z[1], B[0], C[0], X[1], Y[1]);
Cell2XMY M3 (B[2], C[2], Z[2], B[1], C[1], X[2], Y[2]);
Cell2XMY M4 (Bout, Cout, Z[3], B[2], C[2], X[3], Y[3]);

endmodule
```

(vi) Write a Verilog test bench to test the correctness of your design for the following input values: {X=1,Y=1}, {X=3, Y=2}, {X=5, Y=1}, {X=4, Y=5}, and {X=15, Y=15}.

```
module D2XMY_Test();

reg [3:0] X, Y;
wire Bout, Cout;
wire [3:0] Z;

D2XMY M1 (Bout, Cout, Z, X, Y);

initial begin
X=4'b0001; Y=4'b0001;
#100 X=4'b0011; Y=4'b0010;
#100 X=4'b0101; Y=4'b0001;
#100 X=4'b0100; Y=4'b0101;
#100 X=4'b1111; Y=4'b1111;
end
endmodule
```

The simulations results are shown below and it is clear that the circuit is implementing the function Z=2*X-Y correctly.