COE 202, Term 142

Digital Logic Design

Assignment# 2 Solution

Due date: Tuesday, March 31

Q.1. It is required to design a combinational circuit that computes the equation Y=3*X, where X is a 4-bit unsigned number.

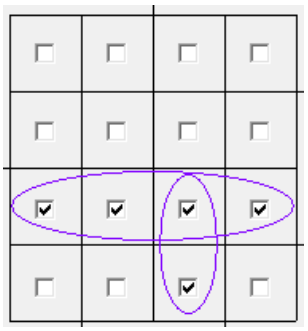
(i) Determine the number of outputs needed for your circuit.

Since the maximum input value is 15, the maximum output value is 3*15=45. Thus, we need 6 outputs.

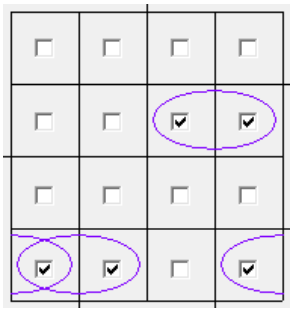
(ii) Derive the truth table of your circuit.

X3	X2	X1	X0	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	0	1	1	0
0	0	1	1	0	0	1	0	0	1
0	1	0	0	0	0	1	1	0	0
0	1	0	1	0	0	1	1	1	1
0	1	1	0	0	1	0	0	1	0
0	1	1	1	0	1	0	1	0	1
1	0	0	0	0	1	1	0	0	0
1	0	0	1	0	1	1	0	1	1
1	0	1	0	0	1	1	1	1	0
1	0	1	1	1	0	0	0	0	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	0	0	1	1	1
1	1	1	0	1	0	1	0	1	0
1	1	1	1	1	0	1	1	0	1

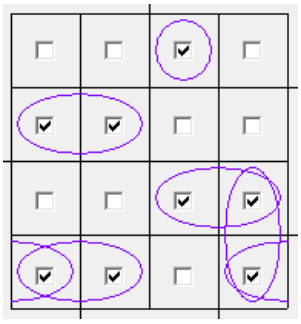
(iii) Derive minimized equations for your circuit using K-Map method.



Y5 = X3 X2 + X3 X1 X0



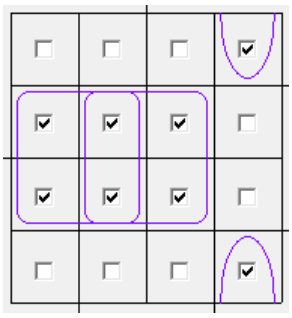
Y4 = X3' X2 X1 + X3 X2' X1' + X3 X2' X0'



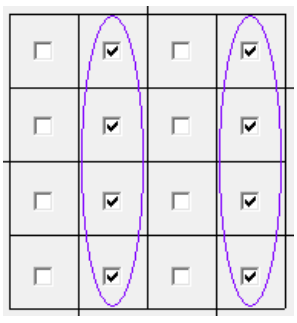
Y3 = X3' X2' X1 X0 + X3' X2 X1' + X3 X2 X1 + X3 X2' X1' + X3 X1 X0'

OR

Y3 = X3' X2' X1 X0 + X3' X2 X1' + X3 X2 X1 + X3 X2' X1' + X3 X2' X0'



Y2 = X2 X1' + X2 X0 + X2' X1 X0'



Y1 = X1' X0 + X1 X0'

Y0 = X0

(iv) Write a Verilog model for modeling your design by using an assign statement for each output.

```
module Times3 (output [5:0] Y, input [3:0] X);

assign Y[5] = X[3] && X[2] || X[3] && X[1] && X[0];

assign Y[4] = !X[3] && X[2] && X[1] || X[3] && !X[2] && !X[1] || X[3] && !X[2] && !X[0];

assign Y[3] = !X[3] && !X[2] && X[1] && X[0] || !X[3] && X[2] && !X[1] || X[3] && X[2] &&
X[1] || X[3] && !X[2] && !X[1] || X[3] && X[1] && !X[0];

assign Y[2] = X[2] && !X[1] || X[2] && X[0] || !X[2] && X[1] && !X[0];

assign Y[1] = !X[1] && X[0] || X[1] && !X[0];

assign Y[0] = X[0];

endmodule;
```

(v) Write a Verilog test bench to test the correctness of your design for the following input values: X=1, X=3, X=5, X=10 and X=15.

```
module t_Times3();
  wire      [5:0] Y;
  reg       [3:0] X;
  Times3 M1 (Y, X);

initial begin
    X=4'b0001;
    #10     X=4'b0011;
    #10     X=4'b0101;
    #10     X=4'b1010;
    #10     X=4'b1111;
end
endmodule;
```