COE 202, Term 121

Digital Logic Design

Assignment# 2

Due date: Sat. Nov. 17

Q.1. Using logic works, you are required to do the following:

a. Model a full adder circuit, verify its correct functionality by simulation. Add delay attributes to the gates by making the delay of a 2-input AND gate 2, the delay of a 2-input OR gate 2 and the delay of an XOR gate 3. Then create a device symbol for it.

b. Using the full adder created in (a) construct a 4-bit Ripple Carry Adder (RCA). Verify its correctness by simulation.

c. Determine theoretically the longest delay in the 4-bit Ripple Carry Adder and verify your result by simulation.

d. Model a 4-bit Carry Look-Ahead Adder (CLA) assuming the delay of an XOR gate is 3 while the delay of other gates is related to its inputs (i.e. the delay of a 2-input AND gate is 2 while the delay the delay of a 3-input AND gate is 3). Verify its correctness by simulation.

e. Determine theoretically the longest delay in the 4-bit Carry Look-Ahead Adder and verify your result by simulation.

Save each part in a separate circuit file. Include snapshots of simulation output to illustrate the correctness of each of your circuits and the maximum propagation delay. Submit your solution as a word document along with the circuits in one zipped file.