

COE 202, Term 112

Digital Logic Design

Assignment# 2

Due date: Sat. April 7

Q.1. Using logic works, you are required to do the following:

- a. Model a full adder circuit, verify its correct functionality by simulation. Add delay attributes to the gates by making the delay of a 2-input AND gate 2, the delay of a 2-input OR gate 2 and the delay of an XOR gate 4. Then create a device symbol for it.
- b. Using the full adder created in (a) construct a 4-bit Ripple Carry Adder (RCA). Verify its correctness by simulation and determine the longest delay.
- c. Model a 4-bit Carry Look-Ahead Adder (CLA) using the same gate delay attributes specified in (a). Verify its correctness by simulation and determine the longest delay. Compare its delay to the 4-bit RCA in (b).

Save each part in a separate circuit file. Include snapshots of simulation output to illustrate the correctness of each of your circuits and the maximum propagation delay. Submit your solution as a word document along with the circuits in one zipped file.