

COE 202, Term 162

Digital Logic Design

Assignment# 2

Due date: Sunday, April 9

- Q.1.** It is required to design an iterative combinational circuit that computes the equation $Z=2*X-Y$, where X and Y are n-bit unsigned numbers.
- (i) Determine the number of inputs and outputs needed for your 1-bit cell.
 - (ii) Derive the truth table of your 1-bit cell.
 - (iii) Derive minimized equations for your 1-bit using K-Map method.
 - (iv) Write a Verilog model for modeling your 1-bit cell by using an assign statement for each output.
 - (v) Write a Verilog model for modeling a 4-bit circuit based on the 1-bit model you have.
 - (vi) Write a Verilog test bench to test the correctness of your design for the following input values: {X=1,Y=1}, {X=3, Y=2}, {X=5, Y=1}, {X=4, Y=5}, and {X=15, Y=15}.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a word file that contains the following items:

- i. Your name and ID
- ii. Assignment number
- iii. Problem statement
- iv. Your solution
- v. Include snapshots of simulation output to illustrate the correctness of your models.