COE 202, Term 142

Digital Logic Design

Assignment# 2

Due date: Tuesday, March 31

Q.1. It is required to design a combinational circuit that computes the equation Y=3*X, where X is a 4-bit unsigned number.

 (i) Determine the number of outputs needed for your circuit.

 (ii) Derive the truth table of your circuit.

 (iii) Derive minimized equations for your circuit using K-Map method.

 (iv) Write a Verilog model for modeling your design by using an assign statement for each output.

 (v) Write a Verilog test bench to test the correctness of your design for the following input values: X=1, X=3, X=5, X=10 and X=15.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a word file that contains the following items:

 i. Your name and ID

 ii. Assignment number

 iii. Problem statement

 iv. Your solution

 v. Include snapshots of simulation output to illustrate the correctness of your models.