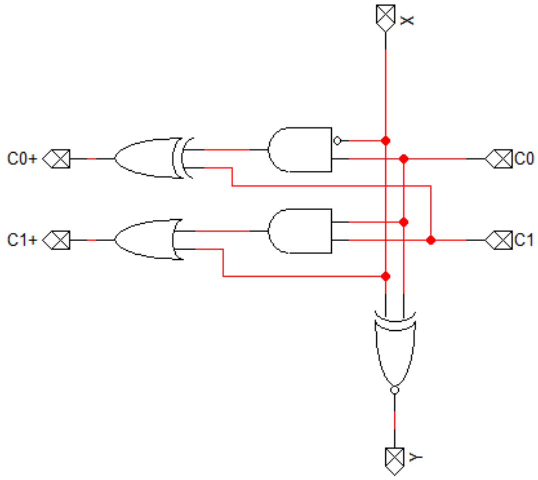
COE 202, Term 162

Digital Logic Design

Assignment# 1 Solution

Due date: Saturday, March 18, 2017

Q.1. Consider the combinational circuit given below which has three inputs C1, C0, and X, three outputs C1+, C0+ and Y:



(i) Write a Verilog model to model the combinational circuit using either primitive gates or assign statement.

```
module Cell3XM1 (output C1P, C0P, Y, input C1, C0, X);

    assign Y = X ~^  C0;

    assign C0P = C1 ^ (~X &  C0);

    assign C1P = X | (C1 &  C0);

endmodule
```

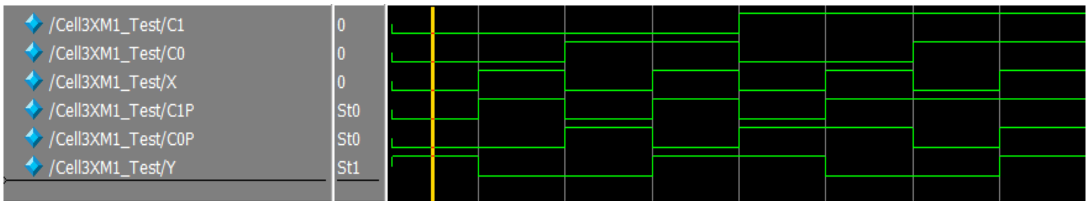
(ii) Write a test bench to test the correctness of your Verilog model by applying all the input patterns to the circuit. Apply consecutive inputs patterns after a delay of 100ps. Verify the correct functionality of your circuit by deriving the truth table and comparing it with what you got from simulations.

```
module Cell3XM1_Test();

reg C1, C0, X;
wire C1P, C0P, Y;

Cell3XM1 M1 (C1P, C0P, Y, C1, C0, X);

initial begin
C1=0; C0=0; X=0;
#100 C1=0; C0=0; X=1;
#100 C1=0; C0=1; X=0;
#100 C1=0; C0=1; X=1;
#100 C1=1; C0=0; X=0;
#100 C1=1; C0=0; X=1;
#100 C1=1; C0=1; X=0;
#100 C1=1; C0=1; X=1;
end
endmodule
```

The expected truth table is as follows:

C1	C0	X	C1P	C0P	Y
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

The simulation waveform given below matches the expected values shown in the truth table.



```
/Cell3XM1_Test/C1   0
/Cell3XM1_Test/C0   0
/Cell3XM1_Test/X    0
/Cell3XM1_Test/C1P  St0
/Cell3XM1_Test/C0P  St0
/Cell3XM1_Test/Y    St1
```

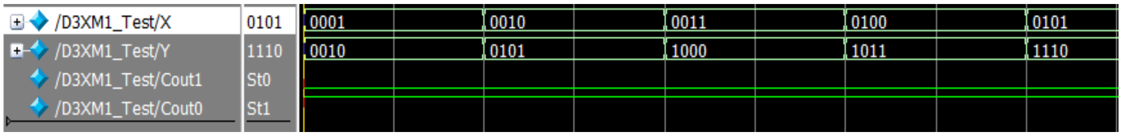
(iii) Write a Verilog model that instantiates four copies of this circuit and connects C1 and C0 of the first instance to 00, C1+ and C0+ of the first instance to C1 and C0 of the 2nd instance, C1+ and C0+ of the 2nd instance to C1 and C0 of the 3rd instance, and C1+ and C0+ of the 3rd instance to C1 and C0 of the 4th instance.

```
module D3XM1 (output Cout1, Cout0, output [3:0] Y, input [3:0] X);

wire  [2:0] C1P, C0P;

Cell3XM1 M1 (C1P[0], C0P[0], Y[0], 0, 0, X[0]);
Cell3XM1 M2 (C1P[1], C0P[1], Y[1], C1P[0], C0P[0], X[1]);
Cell3XM1 M3 (C1P[2], C0P[2], Y[2], C1P[1], C0P[1], X[2]);
Cell3XM1 M4 (Cout1, Cout0, Y[3], C1P[2], C0P[2], X[3]);

endmodule
```

(iv) Write a test bench that tests the 4-bit circuit modeled in (iii) that applies the following input patterns to your circuit (X3X2X1X0)={0001, 0010, 0011, 0100, 0101} and observes the obtained outputs Y3Y2Y1Y0. Can you guess the functionality of the 4-bit circuit?

```
module D3XM1_Test();

reg [3:0] X;
wire Cout1, Cout0;
wire [3:0] Y;

D3XM1 M1 (Cout1, Cout0, Y, X);

initial begin
X=4'b0001;
#100 X=4'b0010;
#100 X=4'b0011;
#100 X=4'b0100;
#100 X=4'b0101;
end
endmodule
```

The simulations results are shown below and it can be deduced from simulations that the circuit is computing the function Y=3*X-1.



```
/D3XM1_Test/X      0101  0001  0010  0011  0100  0101
/D3XM1_Test/Y      1110  0010  0101  1000  1011  1110
/D3XM1_Test/Cout1  St0
/D3XM1_Test/Cout0  St1
```