COE 202, Term 151

Digital Logic Design

Assignment# 1 Solution

Due date: Tuesday, Sep. 29, 2015

Q.1. It is required to design a combinational circuit that has three inputs A, B, and C and a single output Y such that the output is set to 1 if the three inputs are equal to each other.

(i) Derive the equation of the circuit as a sum-of-products equation.

Y= ABC + A'B'C'

(ii) Write a Verilog model to model the gate level design of the circuit using the primitive gates: AND, OR, and NOT gates. Model the delay of each gate as a function of its input i.e., the delay of a NOT gate is 1ps, the delay of a 2-input gate is 2ps, and the delay of a 3-input gate is 3ps.

```
module FirstModule (output Y, input A,B,C);

    and#3(r1,A,B,C);
    not#1(n1,A);
    not#1(n2,B);
    not#1(n3,C);
    and#3(r2,n1,n2,n3);
    or#2(Y,r1,r2);

endmodule
```

(iii) Determine the longest delay of your circuit.

The longest delay is 6 ps.
1 for the inverter + 3 for the 3-input AND gate + 2 for the OR gate = 6.

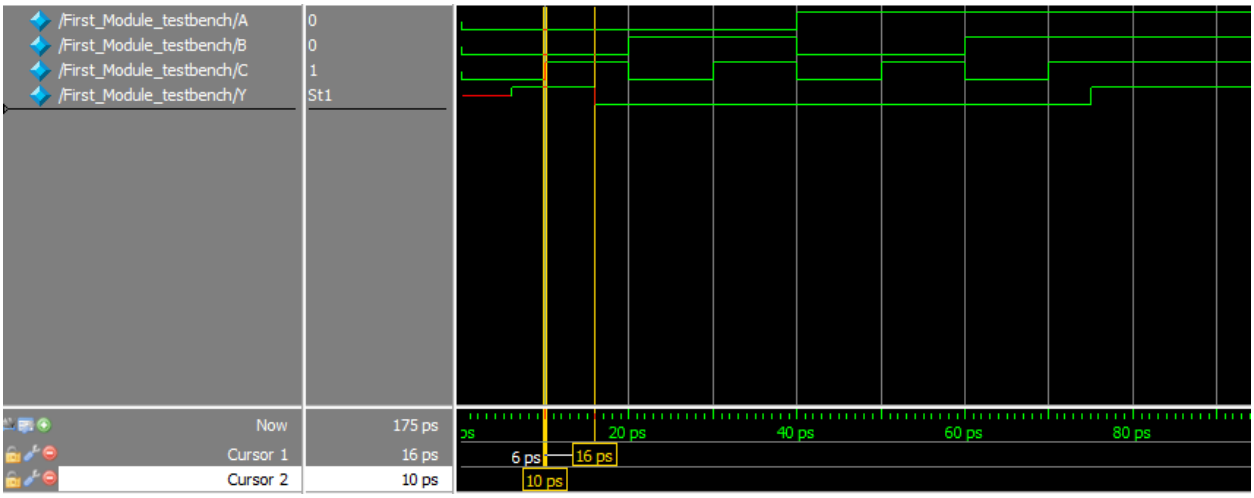
(iv) Write a test bench to test the correctness of your Verilog model by applying all the possible input patterns. Apply consecutive inputs patterns after a delay of 10ps. Verify the correctness of your computed longest delay in (iii).

```
module First_Module_testbench();
    wire Y;
    reg A, B, C;
    FirstModule  M1 (Y, A, B, C);

    initial begin
```

```
 A=0; B=0; C=0;
 #10      A=0; B=0; C=1;
#10       A=0; B=1; C=0;
 #10      A=0; B=1; C=1;
 #10      A=1; B=0; C=0;
 #10      A=1; B=0; C=1;
 #10      A=1; B=1; C=0;
 #10      A=1; B=1; C=1;
end

endmodule
```



(v) Write a second Verilog model to model the circuit using the assign statement to model the equation of the circuit. Use your computed delay in (iii) as the delay of your circuit.

```
module SecondModule(output Y, input A,B,C);

    assign#6 Y = (A & B & C) | (~A & ~B & ~C);

endmodule
```

(vi) Use the test bench in (iv) to test the correctness of your second Verilog model.

```
module second_module_testbench();
    wire Y;
    reg A, B, C;
    SecondModule M2 (Y, A, B, C);

    initial begin
    A=0; B=0; C=0;
    #10      A=0; B=0; C=1;
    #10      A=0; B=1; C=0;
```

```
#10      A=0; B=1; C=1;
#10      A=1; B=0; C=0;
#10      A=1; B=0; C=1;
#10      A=1; B=1; C=0;
#10      A=1; B=1; C=1;
end

endmodule
```