COE 202, Term 142

Digital Logic Design

Assignment# 1 Solution

Due date: Tuesday, March 10, 2015

Q.1. It is required to design a combinational circuit that computes the majority value of the three inputs A, B, and C. If at least two of the inputs have a value of 1, the circuit will produce a value of 1, otherwise it will produce a value of 0.

(i) Derive the equation of the majority circuit as a sum-of-products equation.

M = A B + A C + B C

(ii) Write a Verilog model to model the gate level design of the majority circuit using primitive gates i.e., AND, OR, and NOT gates. Model the delay of each gate as a function of its input i.e., the delay of a NOT gate is 1ps, the delay of a 2-input gate is 2ps, and the delay of a 3-input OR gate is 3ps.

```
module Maj1 (output M, input A, B, C);

and #2 (t1, A, B);
and #2 (t2, A, C);
and #2 (t3, B, C);
or  #3 (M, t1, t2, t3);

endmodule;
```

(iii) Determine the longest delay of your circuit.

The longest delay is 5 ps.

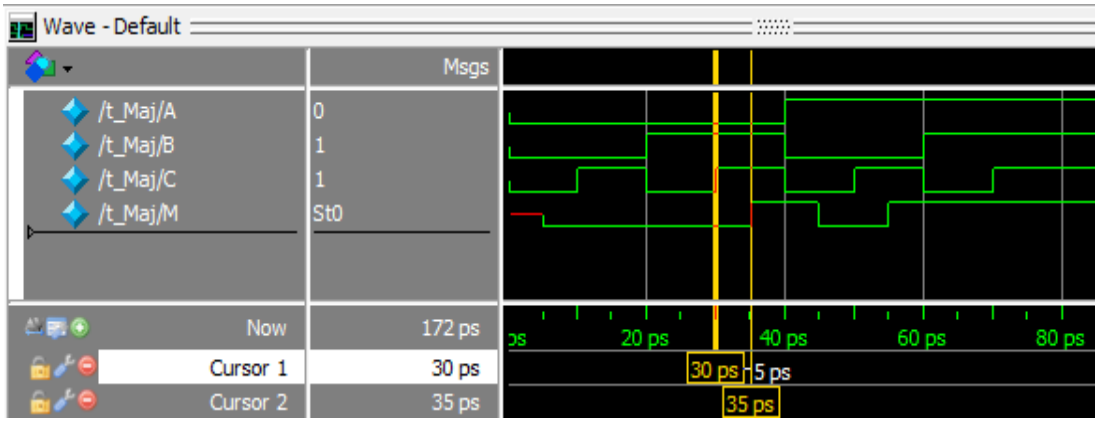
(iv) Write a test bench to test the correctness of your Verilog model by applying all the possible input patterns. Apply consecutive inputs patterns after a delay of 10ps. Verify the correctness of your computed longest delay in (iii).

```
module t_Maj();
  wire      M;
  reg       A, B, C;
  Maj1 M1 (M, A, B, C);

initial begin
   A=0; B=0; C=0;
```

```
  #10      A=0; B=0; C=1;
  #10      A=0; B=1; C=0;
  #10      A=0; B=1; C=1;
  #10      A=1; B=0; C=0;
  #10      A=1; B=0; C=1;
  #10      A=1; B=1; C=0;
  #10      A=1; B=1; C=1;
 end

endmodule
```



(v) Write a second Verilog model to model the majority gate circuit using the assign statement to model the equation of the circuit. Use your computed delay in (iii) as the delay of your circuit.

```
module Maj2 (output M, input A, B, C);

assign #5 M = A && B || A && C || B && C;

endmodule;
```

(vi) Use the test bench in (iv) to test the correctness of your second Verilog model.

```
module t_Maj2();
  wire      M;
  reg       A, B, C;
  Maj2 M1 (M, A, B, C);

initial begin
   A=0; B=0; C=0;
  #10      A=0; B=0; C=1;
  #10      A=0; B=1; C=0;
  #10      A=0; B=1; C=1;
  #10      A=1; B=0; C=0;
  #10      A=1; B=0; C=1;
  #10      A=1; B=1; C=0;
```

```
    #10       A=1; B=1; C=1;
  end

endmodule
```