

COE 202, Term 131

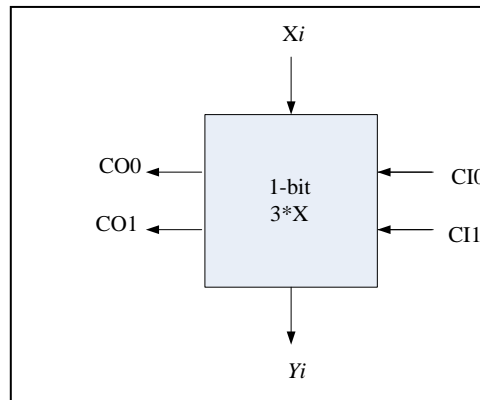
Digital Logic Design

Assignment# 1 Solution

Due date: Tuesday, Nov. 12

Q.1. It is required to design a combinational circuit that computes the equation  $Y=3*X$ , where  $X$  is an n-bit unsigned number.

- (i) Design the circuit as a modular circuit where each module receives a single bit of the input,  $X_i$ .



- (ii) Derive the truth table of your 1-bit module in (i).

Truth Table :

$X_i$	$CI_1$	$CI_0$	$CO_1$	$CO_0$	$Y_i$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	x	x	x
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	x	x	x

(iii) Derive minimized two-level sum-of-product equations for your 1-bit module circuit.

		$C_1 C_0$			
$x_i$		00	01	11	10
0		0	0	X	0
1		0	1	X	1

$$C_{01} = x_i C_1 + x_i C_0$$

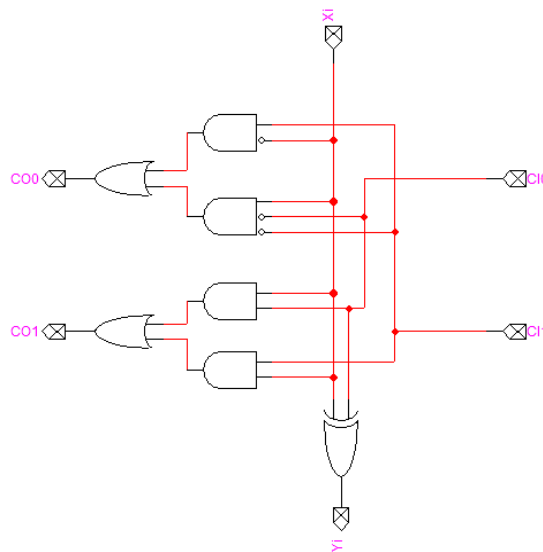
		$C_1 C_0$			
$x_i$		00	01	11	10
0		0	0	X	1
1		1	0	X	0

$$C_{00} = \bar{x}_i C_1 + x_i \bar{C}_1 \bar{C}_0$$

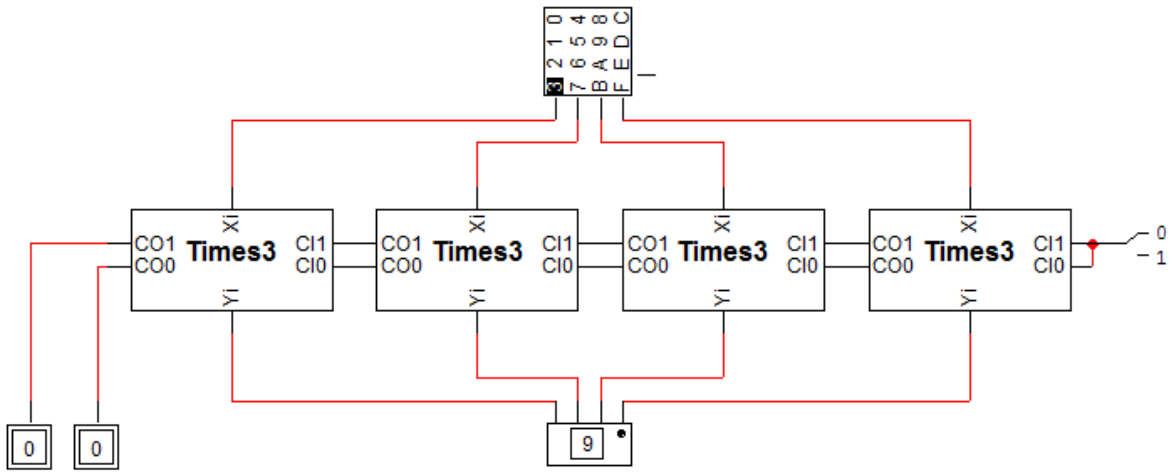
		$C_1 C_0$			
$x_i$		00	01	11	10
0		0	1	X	0
1		1	0	X	1

$$y_i = \bar{x}_i C_0 + x_i \bar{C}_0$$

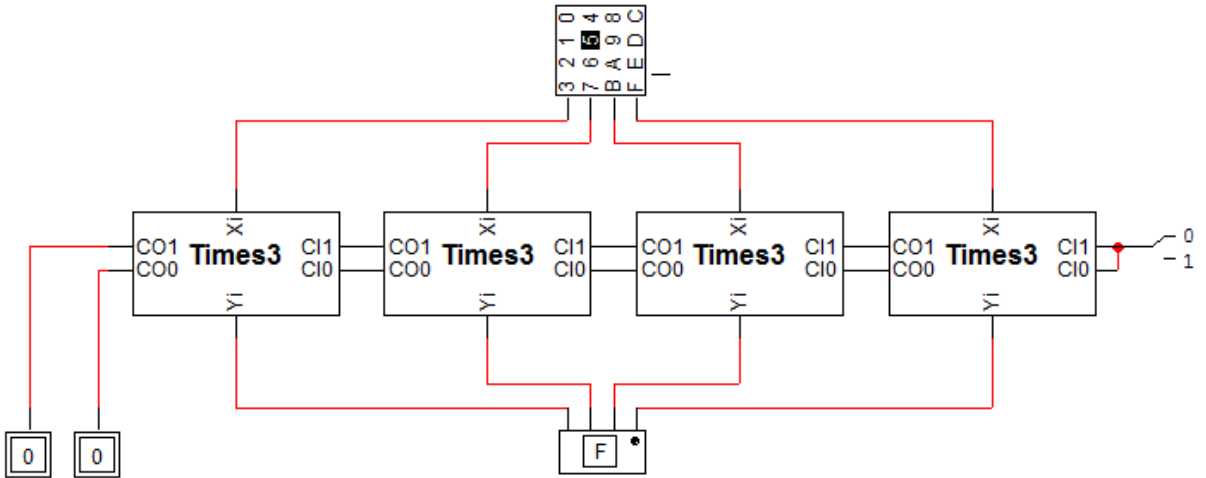
(iv) Verify the correctness of your design by modeling and simulating a 4-bit circuit using LogicWorks.



$$3 \times 3 = 9$$



$$5 \times 3 = 15$$



$$11 \times 3 = 33$$

