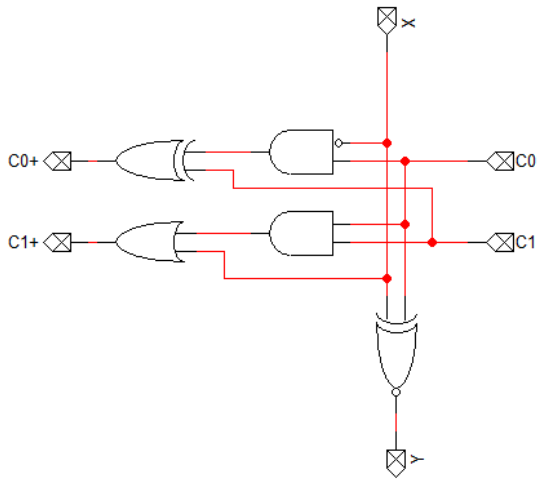
COE 202, Term 162

Digital Logic Design

Assignment# 1

Due date: Saturday, March 18, 2017

Q.1. Consider the combinational circuit given below which has three inputs C1, C0, and X, three outputs C1+, C0+ and Y:



(i) Write a Verilog model to model the combinational circuit using either primitive gates or assign statement.

(ii) Write a test bench to test the correctness of your Verilog model by applying all the input patterns to the circuit. Apply consecutive inputs patterns after a delay of 100ps. Verify the correct functionality of your circuit by deriving the truth table and comparing it with what you got from simulations.

(iii) Write a Verilog model that instantiates four copies of this circuit and connects C1 and C0 of the first instance to 00, C1+ and C0+ of the first instance to C1 and C0 of the 2nd instance, C1+ and C0+ of the 2nd instance to C1 and C0 of the 3rd instance, and C1+ and C0+ of the 3rd instance to C1 and C0 of the 4th instance.

(iv) Write a test bench that tests the 4-bit circuit modeled in (iii) that applies the following input patterns to your circuit (X3X2X1X0)={0001, 0010, 0011, 0100, 0101} and observes the obtained outputs Y3Y2Y1Y0. Can you guess the functionality of the 4-bit circuit?

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***pdf file*** *that contains the following items:*

i. *Your name and ID*
ii. *Assignment number*
iii. *Problem statement*
iv. *Your solution*
v. Include snapshots of simulation output to illustrate the correctness of your models.