COE 202, Term 151

Digital Logic Design

Assignment# 1

Due date: Tuesday, Sep. 29, 2015

Q.1. It is required to design a combinational circuit that has three inputs A, B, and C and a single output Y such that the output is set to 1 if the three inputs are equal to each other.

(i) Derive the equation of the circuit as a sum-of-products equation.

(ii) Write a Verilog model to model the gate level design of the circuit using the primitive gates: AND, OR, and NOT gates. Model the delay of each gate as a function of its input i.e., the delay of a NOT gate is 1ps, the delay of a 2-input gate is 2ps, and the delay of a 3-input gate is 3ps.

(iii) Determine the longest delay of your circuit.

(iv) Write a test bench to test the correctness of your Verilog model by applying all the possible input patterns. Apply consecutive inputs patterns after a delay of 10ps. Verify the correctness of your computed longest delay in (iii).

(v) Write a second Verilog model to model the circuit using the assign statement to model the equation of the circuit. Use your computed delay in (iii) as the delay of your circuit.

(vi) Use the test bench in (iv) to test the correctness of your second Verilog model.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***word file*** *that contains the following items:*

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.