

# **Design and Implementation of Interconnect Efficient Low Density Parity Check Error Correcting Codes**

A Research Proposal Submitted for  
SABIC/Fast Track Research Grants

By

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## Abstract

Forward Error Correcting (FEC) codes are an essential component of modern state-of-the-art digital communication and storage systems. The two leading families of FEC codes are widely considered to be Turbo codes and Low Density Parity Check codes (LDPCs), as they demonstrate performance very close to the information-theoretic bounds predicted by Shannon theory. Recently, the trend in error correcting code implementation is focused on using custom chips for codecs. This is motivated by the need to maximize performance and reduce power dissipation by the codecs. Turbo codes are hard to parallelize, and hence, benefit less from hardware implementation. LDPC codes, however, are parallelizable, and current advances in VLSI technology enables the implementation of their codecs over fairly large code word sizes. Most of LDPC code designs are based on random code generation which results in long interconnect wires. Long interconnect wires increase the load capacitance resulting in slower designs and higher power dissipation. In addition, random code designs result in interconnect routing congestion which reduces the chip area utilization. In this work, we will investigate the design of LDPC codes that are interconnect efficient resulting in high speed designs with low power consumption and maximum chip area utilization due to lower routing congestion.

## 1. Introduction

Forward Error Correcting (FEC) codes are an essential component of modern state-of-the-art digital communication and storage systems. Indeed, in many of the recently developed standards, FEC codes play a crucial role for improving the error performance capability of digital transmission over noisy interference-impaired communication channels. For example, Turbo Codes [1] are adopted for 3<sup>rd</sup> generation mobile cellular systems (CDMA2000/UMTS) and broadband wireless fixed access systems (IEEE 802.16), while Reed-Solomon [1] codes are used in digital versatile storage disks (DVDs). Also, Low Density Parity Check (LDPC) codes [2] have been selected for the next-generation digital satellite broadcasting standard (DVB-S2), ultra high-speed Local Area Networks (10Gbps Ethernet LANs) and are being considered for systems as well.

The two leading families of FEC codes are widely considered to be Turbo codes [1] and Low Density Parity Check codes (LDPCs) [2], as they demonstrate performance very close to the information-theoretic bounds predicted by Shannon theory, while at the same time having the distinct advantage of low-complexity, near-optimal iterative decoding.

Recently, the trend in error correcting code implementation is focused on using custom chips for codecs. This is motivated by the need to maximize performance and reduce power dissipation by the codecs. This is particularly true for coding schemes which can use the parallelism offered by hardware: by using more devices, frequency can be reduced, and voltage scaled, thereby achieving the same throughput for less power [3]. Turbo codes are hard to parallelize [4], and hence, benefit less from hardware implementation. LDPC codes, however, are parallelizable, and current advances in VLSI technology enables the implementation of their codecs over fairly large code word sizes.

Most of LDPC code designs are based on random code generation which results in long interconnect wires. Long interconnect wires increase the load capacitance resulting in slower designs and higher power dissipation. In addition, random code design result in interconnect routing congestion which reduces the chip area utilization. In [5], based on a parallel implementation of LDPC codes, it is reported that routing congestion has resulted in 50% chip area utilization and that most of the power dissipation is due to the switching activity of the long interconnect wires.

In this work, we are interested in designing LDPC codes that are interconnect efficient resulting in high speed designs with low power consumption and maximum chip area utilization due to lower routing congestion.

## **2. Overview of LDPC Codes**

Low Density Parity Check (LDPC) codes are being re-discovered and undergoing a lot of active research after their original introduction by Gallager [2] some forty years

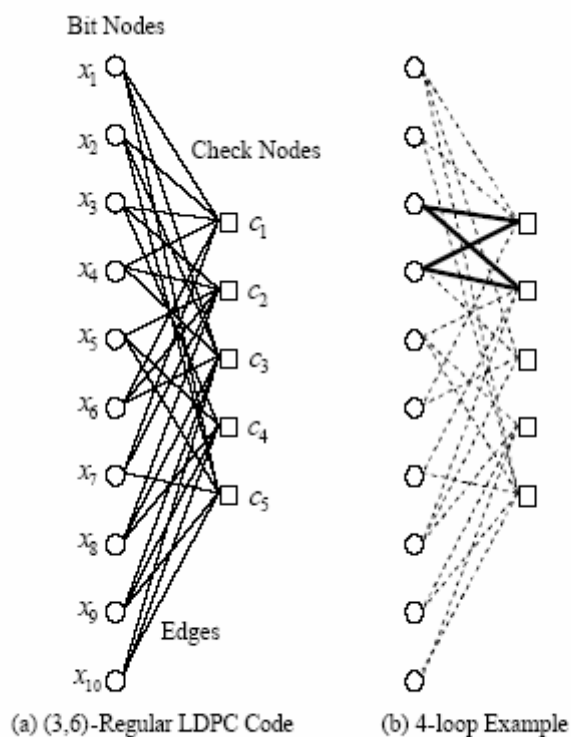
ago. A tutorial review of the work of Gallager that highlights the powerful, capacity-achieving performance of LDPC codes can be found in [6]. Recent advances in LDPC code design have also demonstrated special classes of codes that are shown to outperform their main competitors, namely the powerful state-of-the-art Turbo Codes, for the same block size and code rate [9]. LDPC codes that essentially achieve theoretical capacity limits (with very long block lengths) have also been constructed [12]. Moreover, LDPC codes enjoy the added advantage of a highly parallelizable decoding structure, which makes them well suited for efficient hardware implementation. It should be pointed out, however, that these outstanding performance results are only achievable when the code block length becomes very large (an observation well in line with information theory projections), but nonetheless, a major advantage of LDPC codes is the existence of near-optimal low-complexity decoding algorithms based on iterative probabilistic message passing (or belief propagation), as will be described in the following sections.

In general, LDPC codes can be considered as a class of linear block codes, with their main characteristic being the use of a very sparse, random-like parity-check matrix (having very small column and row weights compared to the code block length). An LDPC code can also be represented by a bi-partite factor graph, which contains two types of nodes: the *code bit nodes* and the *parity check nodes*, interconnected by edges whenever a given check bit appears in the parity check equation of the corresponding information bit. An example of a rate 1/2 LDPC code with block size 10 is given by the following 5x10 parity check matrix  $\mathbf{H}$  (although this is not really a sparse matrix, for this simple illustrative example), and the corresponding code graph is illustrated in the figure below.

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

This particular example corresponds to a class of LDPC codes known as *regular* LDPC codes, for which all nodes of a given type (whether bit nodes or check nodes)

have the same degree which corresponds to the number of graph edges connected to that node. The example illustrated above is classified as a (3,6) regular LDPC code, since every bit node has degree 3, and every check node has degree 6. Recently, more powerful LDPC code constructions known as *irregular* LDPC codes [8, 9] have been introduced and shown to achieve better performance than regular codes. These irregular LDPC codes do not impose the constraint of having the same degree of connectivity for every bit and check node, and they have been shown to achieve near-capacity performance (also out-performing turbo codes), as discussed in [9].



**Figure 1 LDPC Code Graph Example.**

An important feature that impacts LDPC code performance is the presence of so-called loops (or closed paths) on the code's graph. Loops (and particularly the shortest ones, of length 4) hinder the performance of the iterative decoding algorithm (to be discussed next) and therefore result in poor error performance. An example of a 4-loop from the code's matrix given above is shown in Figure 1.

Another feature of LDPC codes is the need for the encoding operation to transform  $\mathbf{H}$  into systematic form to obtain the generator matrix  $\mathbf{G}$ . The technique of Gaussian elimination is typically used for this operation. However, this operation usually destroys the sparse nature of the original  $\mathbf{H}$  matrix, and therefore yields costly storage and computing requirements for the LDPC encoder. In fact, one of the aspects of LDPC codes that is perceived to adversely affect their excellent performance is the “complex encoding” process, in contrast with the straightforward encoding of convolutional and turbo codes for example. However, recent contributions [11, 13] have shown that LDPC codes are also amenable to simple encoding structures without sacrificing decoder error performance.

These aspects, in combination with the highly efficient low-complexity sum-product message passing decoding algorithm (to be discussed next), give LDPC codes a distinct advantage over turbo codes, their main competitors, and this is one of the main motivations for the proposed research work.

### 3. Iterative Decoding of LDPC Codes

Similar to turbo codes, LDPC decoding is also developed within the framework of iterative decoding principles, with the main feature of exchanging *soft* information between successive iterations. An efficient iterative message-passing algorithm known as the belief propagation algorithm [7], also known as the sum-product algorithm, is typically used for the decoding of LDPC codes, and is shown to be closely approximate optimal maximum likelihood decoding [2, 6].

In the following, we give a brief description of this algorithm, mainly using the notation and terminology of [6]. We also note that there is a well-known, computationally efficient log-domain implementation of the sum-product LDPC decoding algorithm which we don't discuss here for the sake of brevity (see, for example, [14]).

In the subsequent description, the elements of a codeword  $\mathbf{c}$  are referred to as bits, and the rows of the parity matrix  $\mathbf{H}$  are designated as checks. The set of bits  $l$  that participate in check  $m$  is denoted by  $L(m) = \{l : H_{ml} = 1\}$ . Similarly, the set of checks

in which bit  $l$  participates is denoted by  $M(l) = \{m : H_{ml} = 1\}$ . Also, a set  $L(m)$  in which bit  $l$  is excluded is denoted by  $L(m) \setminus l$ , and likewise for  $M(l) \setminus m$  which refers to  $M(l)$  not including check  $m$ . The decoding algorithm has two alternating parts in which quantities  $q_{ml}$  and  $r_{ml}$  associated with each nonzero element of  $\mathbf{H}$  are iteratively updated. The quantity  $q_{ml}^i$  can be thought of as the probability information that the bit node  $l$  sends to the check node  $m$  indicating  $\text{Prob}(x_l = i)$  with  $i=0, 1$ . On the other hand, the quantity  $r_{ml}^i$  is meant to be the probability information that the  $m$ th check node gathers about the  $l$ th bit of  $\mathbf{x}$  being  $x_l = i$  when the other bits have probabilities given by  $\{q_{ml'} : l' \in L(m) \setminus l\}$ . The belief propagation algorithm is shown to converge to the actual posterior probabilities of the received bits if the bipartite graph associated with the underlying parity matrix  $\mathbf{H}$  has no cycles [6, 7]. In the following, we briefly summarize the algorithm steps.

**1. Initialization:** The variables  $q_{ml}^0$  and  $q_{ml}^1$  are initialized to the probabilities  $p_l^0$  and  $p_l^1$  that code bit  $x_l$  is zero or one, respectively. For memoryless symmetric channels model with binary input bits  $x_l$  and continuous channel output  $y_l$ , these probabilities are given by  $p_l^i = P(y_l | x_l = i)$ , where  $i = 0, 1$ . For every position  $(m, l)$  in the matrix  $\mathbf{H}$  where the entry is non-zero (i.e.,  $H_{ml} = 1$ ), we have the following initialization:  
 $q_{ml}^i = p_l^i$ .

**2. Horizontal Step (Checks to Bits):** Each check node  $m$  gathers all the incoming information  $q_{ml}^i$ , and updates the belief on the  $l$ th bit based on all other bits that participate in check equation  $m$ .

$$r_{ml}^i = \sum_{x_{l'} : l' \in L(m) \setminus l} P(\{x_{l'}\} | x_l = i, \mathbf{H}) \times \prod_{l' \in L(m) \setminus l} q_{ml'}^{x_{l'}}$$

for  $i=0,1$ . Notice that the exclusion of the term  $q_{ml}$  in the computation of  $r_{ml}$  is necessary in order to only include “extrinsic” information about the  $l$ th bit from the  $m$



parity check equation. In the above expression, the function  $P(\{x_r\} | x_l = i, \mathbf{H})$  is an indicator function given by:

$$P(\{x_r\} | x_l = i, \mathbf{H}) = \begin{cases} 1, & \text{if } \sum \oplus \{x_r, i\} = 0 \\ 0, & \text{otherwise} \end{cases}$$

where  $\sum \oplus$  represents a modulo-2 summation.

**3. Vertical Step (Bits to Checks):** The computed values of  $q_{ml}^i$  are used to update the information (or belief) that each bit node  $l$  propagates back to check node  $m$ . In doing so, the information coming from check node  $m$  itself should not be included. We thus have

$$q_{ml}^i = \alpha_{ml} p_l^i \prod_{m' \in M(l) \setminus m} r_{m'l}^i$$

for  $i=0,1$ . The term  $\alpha_{ml}$  is used as a normalization factor to ensure  $q_{ml}^0 + q_{ml}^1 = 1$ .

Each node bit  $l$  collects probability information from the check nodes that connect to it, and updates its a posteriori probabilities (APP) through the following expressions:

$$q_l^i = \alpha_l p_l^i \prod_{m \in M(l)} r_{ml}^i$$

for  $i=0,1$ . The normalization factor  $\alpha_l$  is chosen such that

$q_l^0 + q_l^1 = 1$ . Notice that two components contribute to the APP terms: the intrinsic information from  $p_l$ , and an extrinsic part through the  $r_{ml}$  terms.

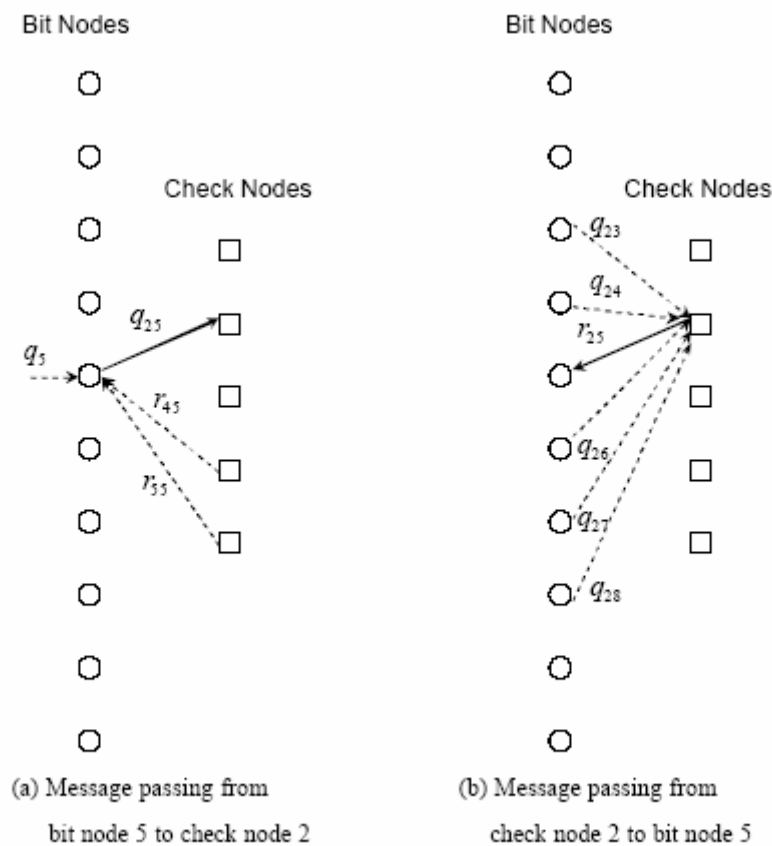
After each vertical-horizontal iteration, a hard decision is made on each bit APP  $q_l$ , resulting in a tentative decoded vector  $\hat{x}$ . This is then used to decide whether to stop the decoding algorithm as outlined next.

**4. Stopping Criterion:** The decoded vector  $\hat{x}$  is used to check whether it satisfies  $H\hat{x} = 0$ , in which case it is declared as a valid codeword. If not, iterative

decoding continues from Step 2 above until it is eventually successful, or a preset number of maximum iterations is reached.

It should also be noted that any failed decoding is automatically detected. That is, the belief propagation decoding of LDPC codes gives error detection for free, unlike turbo or convolutional codes which require a separate additional mechanism for error detection. An illustration of the iterative LDPC belief propagation decoding algorithm is shown in Figure 2 below.

It is also possible to implement this algorithm in the log-domain, thus resulting in further computational simplifications (because all multiplicative operations are transformed into additions, which are simpler to implement in hardware). In addition, the structure of the decoding algorithm is highly amenable to efficient hardware parallelization (which would greatly benefit system throughput), and this will be further explored in the proposed work.



**Figure 2 Illustration of LDPC Decoding by Message Passing.**

## 4. LDPC Code Design: a Hardware-Oriented Perspective

There are several approaches that have recently been proposed to design good LDPC codes. Basically, the classical design approaches can broadly be classified as: 1) deterministic constructions based on finite geometries and graph-theoretic concepts to obtain good distance and cycle properties for the codes [23,24], and 2) pseudo-random constructions for girth conditioning aided by computer search/simulations to obtain parity check matrices giving good error performance [21,22]. Other researchers have also looked at the LDPC encoder design aspects, since the encoder for purely random parity check matrices can be complex compared to competing FEC schemes, and efficient solutions were proposed in [13,20]. All these preceding approaches address the problem of code design from the point of view of error performance optimization. However, another equally important aspect (that didn't receive as much attention in the literature) is related to the hardware implementation issues (particularly in VLSI), and it is this aspect of code design that is the guiding motivation of this proposed research.

Some of the recent contributions in this regard are found in [15, 16] where LDPC codes are designed based on special families of graphs (e.g., Ramanujam graphs) which impose constraints on the code parameters. In [17], simulated annealing is used to generate LDPC graphs satisfying certain conditions. In [18], the bit-filling method is proposed to generate LDPC graphs given constraints on the degree of the nodes and the girth (length of the smallest cycle in a bipartite graph). In [19], an algorithm is proposed to generate LDPC codes with a bound on the 'height' of the VLSI layout of the decoder. It is shown that this approach limits the routing congestion with little impact on error correcting capability of the code.

Practical implementations of error correction algorithms are evaluated by cost (silicon area), power, throughput, latency, flexibility and scalability. Some LDPC research that promise very good error performance, very close to Shannon limit, resulted in complex code structures that are not practical for implementation.

In implementing a LDPC decoder, we have to consider two main requirements: message computation and exchange of message between nodes. The later should be

considered when constructing a LDPC code. The message computation is usually expressed in log-probability domain since it replaced multipliers with adders. Although working in the log-probability domain simplifies the evaluation of products, it requires lookup tables to evaluate the functions.

A major requirement that should be fulfilled by a LDPC decoder is to provide an interconnect network to facilitate message passing between check and bit nodes. Each edge in a Tanner Graph defines a path of a message passing between two nodes. Direct wiring of the interconnect network may lead to congestion due to disorganized nature of the LDPC graph. This problem can be partially solved by using memory, or in other words by making the structure of the decoder serial instead of being fully parallel.

Two main classes of decoder architectures exist: parallel and serial. Parallel decoders directly map the nodes of the graph onto processing elements, and the edges of the graph onto an interconnect network. This approach will fully utilize the inherent parallelism of the decoding algorithm and it will be throughput-efficient but with the expense of requiring larger area. On the other hand, serial architectures distribute the arithmetic requirements sequentially among small number of processing elements. This approach requires fewer processing elements but it will also need additional memory elements.

In [5], a 1024-bit, rate= $1/2$  LDPC code fully parallel decoder with the maximum symbol throughput of 1 Gbit/s has been implemented using ASIC technology. The ASIC LDPC decoder [5] with only 1K-bit code length consumed 1.7M gates with a high routing overhead resulting in 50% chip utilization due to the randomness of the LDPC code interconnections.

A high-performance parallel implementations of an encoder and decoder for the Parallely Concatenated Parity Check (PCPC) class of LDPC codes [32] was presented in [33]. The designs are based on a code rate of  $8/9$ , a block size of 576 bits and a (6, 2) finite-precision implementation. The Bit Error Rate (BER) performance has been shown to be very close to that for a hypothetical floating-point implementation of the same architecture.

In [25], a joint code and decoder design methodology was proposed for (3,  $k$ )-regular LDPC code and partly parallel decoder design to achieve appropriate trade-offs

between hardware complexity and decoding throughput. Based on applying the joint code and decoder design methodology [25], a high-speed  $(3, k)$ -regular LDPC code partly parallel decoder architecture was developed in [26], based on which a 9216-bit, rate= $1/2$   $(3, 6)$ -regular LDPC code decoder was implemented on Xilinx FPGA device. With a maximum of 18 iterations for each code block decoding, this partly parallel decoder supported a maximum symbol throughput of 54 Mbps and achieved BER  $10^{-6}$  at 2dB over additive white Gaussian noise (AWGN) channel.

In [31], a methodology for the implementation of an LDPC encoder/decoder in a commercial FPGA and a Genetic algorithm that is used to optimize the implementation were presented. The proposed solutions optimized the routing delays in the solutions generated by the Xilinx's tools.

A massively scalable architecture that reduces the decoding latency of an LDPC decoder was proposed in [27]. The architecture uses hardware scaling and memory partitioning to achieve a throughput of 100 Gbps. A pseudo-random construction of the parity check matrix that is specifically designed to facilitate parallelization of the decoder is used.

Different architectures for low-density parity-check (LDPC) decoders are discussed in [28], with methods to reduce their complexity. Serial implementations similar to traditional microprocessor datapaths are compared against implementations with multiple processing elements that exploit the inherent parallelism in the decoding algorithm. Several classes of LDPC codes, such as those based on irregular random graphs and geometric properties of finite fields are evaluated in terms of their suitability for VLSI implementation and performance as measured by bit-error rate.

In [29], the finite precision effects on the decoding performance of LDPC codes were analyzed and several quantization schemes for the received data and extrinsic information for log-BP based LDPC decoder were investigated. It is reported that 4 bits and 6 bits are adequate for representing the received data and extrinsic information, respectively and offer a good tradeoff between performance and hardware complexity.

Fixed point DSP implementation of LDPC decoder was reported in [30]. A simplified decoding algorithm was used and a stopping criteria for the iterative decoder was implemented to reduce the average number of required iterations. This led to an

implementation with increased throughput compared to other implementations of LDPC codes or Turbo codes. The implemented decoder was able to decode at 5.4Mbps on a Texas Instruments TMS320C64xx DSP running at 600MHz.

## 5. Proposed Methodology

In this work, we investigate the design of LDPC codes that result in interconnect efficient decoder implementations. We assume a fully parallel implementation of the LDPC decoder. Our objective is to design LDPC codes with a constraint on the interconnect wire length. This will result in constraining the wire capacitance which has a direct impact on the maximum signal delay in the design and the power dissipation. Furthermore, this will lower the interconnect routing congestion and hence reduces the chip area and maximizes chip utilization.

One approach that will be investigated in this direction is to assume that the bit nodes and check nodes are laid out in a two-dimensional structure as shown in Figure 3. Then, with a given requirement on the degree of bit nodes, connections between each bit node and check nodes will be constrained within a given window of a specified number of rows and columns. This guarantees that the wire length interconnecting a bit node with check nodes is bounded by a maximum length. For example, as shown in Figure 3 for a  $\frac{1}{2}$  rate 32-bit code, bit nodes 19 and 20 with the given constraint window of two rows and three columns can only connect to check nodes 5, 6, 7, 9, 10, and 11 bounded by the specified window. In addition, the code will be designed taking into account the girth of the graph i.e., it will be ensured that the design code has no cycles of a predetermined length e.g. 4. Connections between bit nodes and check nodes will be done randomly as long as they do not violate the specified constraints.

Various LDPC code designs will be investigated based on this approach by varying the constraint window size, the girth of the graph, and the bit and check nodes degrees. The design that results in the best error performance will be chosen.

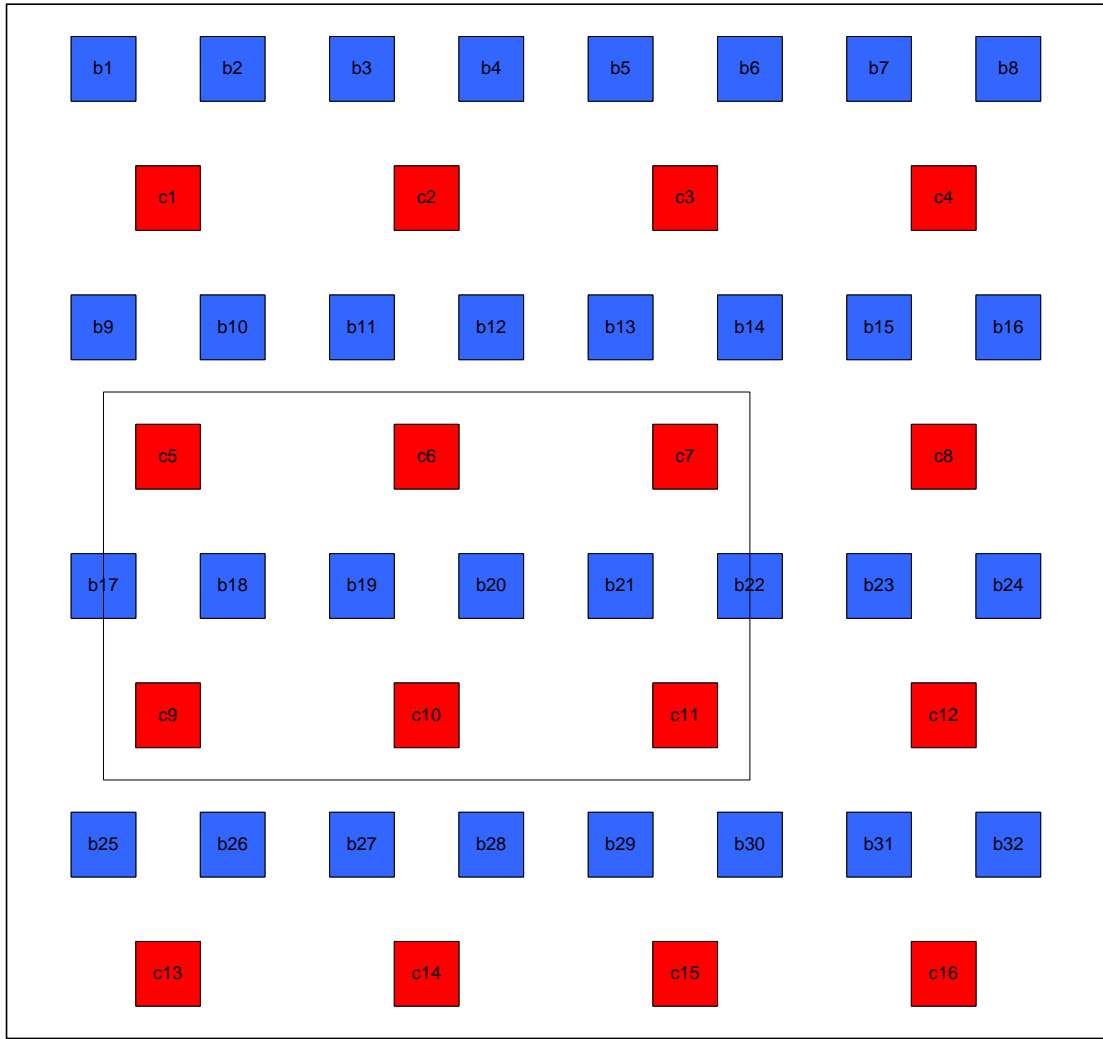
In order to validate the hardware advantage by the window constrained LDPC code design, a general VHDL model for fully parallel implementation of any LDPC code based on the H matrix will be developed. This will allow the use of synthesis tools like Synopsys and Xilinx Synthesis tools to synthesize the designed LDPC code and obtain estimates on area, delay and power dissipation.

Another direction in this work is to investigate the design of scalable LDPC code that has the advantage of being automatically generated for any code size and guarantees a maximum wire length regardless of the code size. The idea is based on designing a basic cell that can be replicated with well defined inter-cell connections that maintain certain properties that are known to correlate with error performance of the code e.g. girth. An example of such a cell is shown in Figure 4, which has 16 bit nodes and 8 check nodes with a girth of 8. The advantage of this approach is that once the code is designed and optimized for performance, it is expected that good properties of the code will be maintained for any code size required. Thus, the design will be scalable as it will maintain the speed irrespective of the code length since the maximum wire length will have the same constraint. This is in contrast to random-based LDPC codes which are expected to have lower performance and higher power dissipation with the increase in the code size due to the expected increase in interconnect wire length.

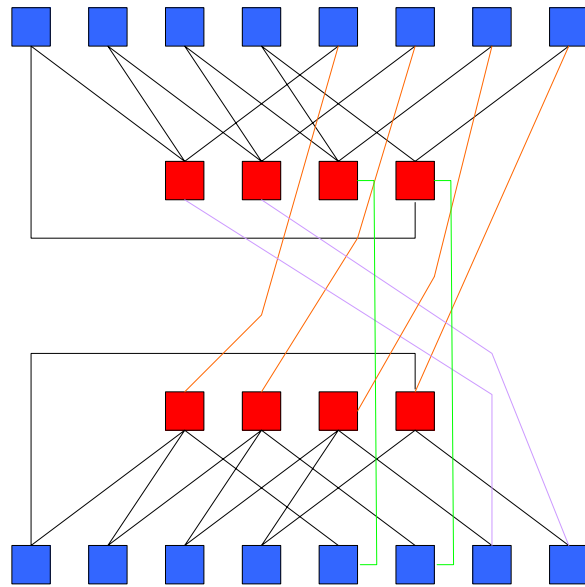
## **6. Project Objectives**

The principle objectives of this project are as follows:

1. Design of interconnect-efficient Low Density Parity Check codes with competitive performance compared to other random-based LDPC codes.
2. Investigate different approaches for LDPC code design taking into consideration performance and implementation complexity (at short to moderate block lengths).
3. Prototype the proposed LDPC code design and verify the efficiency of their implementations using synthesis tools and Field Programmable Gate Arrays (FPGAs).



**Figure 3 Two-dimensional layout of bit nodes and check nodes for 1/2 rate 32-bit LDPC code.**



**Figure 4 An example 16-bit LDPC code cell.**



## 7. Project Schedule

The time span of this project is eighteen (18) months during which eight tasks will be carried out. Table 1 shows a schedule of these tasks indicating the time requirement of each.

Table 1. Work plan timetable

TASK	MONTH								
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18
1. Literature Survey	↔								
2. Investigate different approaches for LDPC code design taking into consideration performance and implementation complexity (at short to moderate block lengths).	↔								
3. Development of random-based LDPC code design tool with girth constraints.		↔							
4. Design of interconnect efficient Low Density Parity Check codes with competitive performance to other random-based LDPC codes.				↔					
5. Comparison of Error performance analysis of proposed designs using simulations.				↔					
6. Prototype the proposed LDPC code design and verify the efficiency of their implementations using synthesis tools and FPGAs.							↔		
7. Progress reports.			↔			↔			
8. Preparing final report and publications.									↔

## **8. Utility Value & Deliverables**

The utility value of this project is many-fold, and includes the following aspects:

1. The results of this research can be used by industry as the designed LDPC codes can offer higher speed, less area and low power than existing designs.
2. The results of this work can be used by other investigators in academia and industry to enhance existing methods.
3. The project provides an opportunity for training graduate students on conducting scientific research.

The deliverables of this project can be summarized as follows:

1. A tool for interconnect efficient LDPC code design that generates the LDPC code based on a given input parameters like code size and node degree and maximum interconnect length.
2. A model in high-level description language (VHDL) than can be used for synthesis and implementation of the LDPC code decoder.

## **9. Monitoring and Evaluation Plan**

The investigators will be involved in all the stages of the project and will work for the whole duration of the project. A graduate student will also assist during the entire duration of the project. The investigators will hold meetings as often as necessary (minimum once a week) to coordinate their work and to make necessary decisions. Periodic progress reports will be submitted every 6 months summarizing the status and accomplishments of the project and a final report documenting the project achievement will be submitted at the end of the project.

## 10. Detailed Budget

### 1. Investigators

Both the principle investigator and co-investigator will work for 18 months during the regular semesters for the entire duration of the project. They will receive payments as per the university regulations. The graduate student(s) will assist in the implementation aspects of the research. His total compensation will be (10,800/- per Graduate Student/Research Assistant).

Dr Aiman El-Maleh (PI)	SR 1,200 X 18 = SR 21,600
Dr. Mohammed Adnan Landolsi (CO-I)	SR 1,000 X 18 = SR 18,000
Graduate Student	SR 600 X 18 = SR 10,800
<hr/>	
Subtotal	SR 50,400

### 2. Equipment, Materials and Charges

Facilities available at KFUPM will be used at no charge to the project. Additional equipment required for the project includes a high quality scanner with an estimated amount of SR 1500/-. Stationary and miscellaneous expenses for consumables such as floppies, CDs, paper, printer toner, etc., will amount to SR 2,000/-, purchase of literature and books, etc., will require SR 2,500/-. A secretary will work for the entire duration of the project. SR 2,000/- for payments to secretary will be required.

Individual items of the budget are summarized below:

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Man Power	SR 50,400/-
Scanner	SR 1,500/-
Books, other literature	SR 2,500/-
Stationary and Miscellaneous	SR 2,000/-

Secretary	SR 2,000/-
Conference Attendance (1 Trip)	SR 10,000/-

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The total cost of the project is estimated to be SR 68,400/-

SR 68,400/-= US \$ 1 18,240/-)

## **Project Researchers' Qualifications:**

**Dr. Aiman El-Maleh** holds a B.Sc. in Computer Engineering, with first honors, from King Fahd University of Petroleum & Minerals in 1989, a M.A.SC. in Electrical Engineering from University of Victoria, Canada, in 1991, and a Ph.D in Electrical Engineering, with dean's honor list, from McGill University, Canada, in 1995.

Dr. El-Maleh is an Assistant Professor in the Computer Engineering Department at King Fahd University of Petroleum & Minerals since September 1998. He was a member of scientific staff with Mentor Graphics Corp., a leader in design automation, from 1995-1998.

Dr. El-Maleh's research interests are in the areas of synthesis, testing, and verification of digital systems. In addition, Dr. El-Maleh has research interests in VLSI design, design automation, and computer arithmetic.

Dr. El-Maleh is the winner of the best paper award for the most outstanding contribution in the field of test for 1995 at the European Design & Test Conference. His paper presented at the 1995 Design Automation Conference was also nominated for best paper award. He holds one US patent.

Dr. El-Maleh was a member of the program committee of the Design Automation and Test in Europe Conference (DATE'98).

**Dr. Mohammed Adnan Landolsi** received his BS from the National Engineering Institute of Tunis in 1988, and the M.S and Ph.D in Electrical Engineering from the University of Michigan in 1991 and 1996, respectively.

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Dr Landolsi has authored and co-authored 4 U.S patents, and over 20 technical publications in international journals and conference proceedings.

## References

- [1] M. Bossert. *Channel Coding for Telecommunications*. John Wiley and Sons, Aug. 1999.
- [2] R. G. Gallager, *Low Density Parity Check Codes*, Cambridge, MA: MIT Press, 1963.
- [3] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-Power CMOS Digital Design,” *IEEE J. Solid-State Circuits*, 27:473{484, Apr. 1992.
- [4] E. Yeo, P. Pakzad, B. Nikolic, and V. Anantharam, “VLSI Architectures for Iterative Decoders in Magnetic Recording Channels,” *IEEE Trans. Magnetics*, 37:748{755, Jan. 2001.
- [5] A. J. Blanksby and C. J. Howland, “A 690-mW 1-Gb/s 1024-b, Rate-1/2 Low-Density Parity-Check Decoder,” *IEEE J. Solid-State Circuits*, 37:404{412, Mar. 2002.
- [6] D.J.C. MacKay, “Good error-correcting codes based on very sparse matrices,” *IEEE Trans. Inform. Theory*, vol.45, pp.399-431, March 1999.
- [7] J. Pearl, *Probabilistic Reasoning in Intelligent Systems: Networks of Plausible Inference*, San Mateo: CA, Morgan Kaufmann, 1988.
- [8] M. Luby *et al*, “Analysis of low density codes and improved designs using irregular graphs,” in *Proc. 30th Annual ACM Symp. Theory of Computing*, pp.249-258, 1998.
- [9] T.J. Richardson, A. ShoroAllahi, and R. Urbanke, “Design of capacity-approaching irregular parity check codes,” *IEEE Trans. Inform. Theory*, vol.47, pp.619-637, Feb. 2000.
- [10] T.J. Richardson and R. Urbanke, “The capacity of low-density parity check codes under message-passing decoding,” *IEEE Trans. Inform. Theory*, vol.47, pp.599-618, Feb. 2000.
- [11] T.J. Richardson and R. Urbanke, “Efficient encoding of low-density parity-check codes,” *IEEE Trans. Inform. Theory*, vol.47, pp.638-656, Feb. 2000.
- [12] S-Y. Chung *et al*, “On the design of low-density parity-check codes within 0.0045 dB of the Shannon limit,” *IEEE Commun. Letters*, vol.5, no.2, pp. 58-60, Feb. 2001.

- [13] S.J. Johnson and S.R. Weller, "A family of irregular LDPC codes with low encoding complexity," *IEEE Commun. Letters*, vol.7, no.2, pp. 79-81, Feb. 2003.
- [14] J.L. Fan, *Constrained Coding and Soft Iterative Decoding*, Boston, MA: Kluwer Academic Publishers, 2001.
- [15] M. Mansour and N. Shanbhag, "Architecture-Aware Low-Density Parity-Check codes," *IEEE Int. Symp. Circuits and Systems*, May 2003.
- [16] M. Mansour and N. Shanbhag, "A Novel Design Methodology for High Performance Programmable Decoder Cores for AA-LDPC Codes," *IEEE Workshop on Signal Processing Systems*, Aug. 2003.
- [17] J. Thorpe, "Design of LDPC Graphs for Hardware Implementation," *IEEE Int. Symp. Inform. Theory*, page 483, Lausanne, Switzerland, June 2002.
- [18] J. Campeliot, D. S. Modha, and S. Rajagopalan, "Designing LDPC Codes Using Bit-Filling," *IEEE Int. Conf. Communications*, pages 55-59, June 2001.
- [19] Marghoob Mohiyuddin, Amit Prakash, Adnan Aziz and Wayne Wolf, "Synthesizing Interconnect Efficient Low Density Parity Check Codes," *Design Automation Conf.*, 2004.
- [20] M. Yang, Y. Li and W.E. Ryan, "Design of Efficiently-Encodable Moderate-Length High-Rate Irregular LDPC Codes," *Proc. Allerton Conf. Comm., Control and Comp.*, Oct. 2002.
- [21] Y. Mao and A. Banihashemi, "A Heuristic Search for Good Low-Density Parity-Check Codes at Low Block Lengths," in *Proc. IEEE Intl. Conf. Comm.*, 2001.
- [22] X. Hu, E. Eleftheriou and D.M Arnold, "Progressive Edge-grown Tanner Graphs," in *Proc. IEEE GlobeCom*, 2001.
- [23] Y. Kou, S.Lin and M.P.C Fossorier, "Low Density Parity Check Codes based on Finite Geometries: A Rediscovery and New Results," *IEEE Trans. Info Theory*, Nov. 2001.
- [24] J. Rosenthal and P.O Vontobel, "Construction of LDPC Codes using Ramanujan Graphs and Ideas from Margulis," in *Proc. Allerton Conf. Comm., Control and Comp.*, Oct. 2000.
- [25] T. Zhang and K. K. Parhi, "VLSI implementation-oriented  $(3, k)$ -regular low-density parity-check codes," *IEEE Workshop on Signal Processing Systems*, Sept. 2001.
- [26] T. Zhang and K. K. Parhi, "A 54 MBPS  $(3, 6)$ -REGULAR FPGA LDPC DECODER," *Proc. IEEE Workshop on Signal Processing Systems*, 2002.



- [27] Anand Selvarathinam, Gwan Choi, Krishna Narayanan, Abhiram Prabhakar, and Euncheol Kim, "A Massively Scaleable Decoder Architecture for Low-Density Parity- Check Codes," *Proc. IEEE ISCAS*, 2003.
- [28] Engling Yeo, Borivoje Nikoli , and Venkat Anantharam, "Architectures and Implementations of Low-Density Parity Check Decoding Algorithms," *IEEE International Midwest Symposium on Circuits and Systems*, 2002.
- [29] T. Zhang, Z. Wang and K. K. Parhi, "On Finite Precision Implementation of Low Density Parity Check Codes Decoder," *Proc. of 2001 IEEE Int. Symp. on Circuits and Systems*, pp. 202-205, 2001.
- [30] G. Lechner, J. Sayir and M. Rupp, "Efficient DSP implementation of an LDPC decoder," *Proc. IEEE Int. Conf. Acoustics, Speech, and Signal Processing*, Volume 4, Page(s):iv-665 - iv-668, 17-21 May 2004.
- [31] D. Barral, W. Falcon, J Altun and R.A. Carrasco, "On the implementation and optimisation of LDPC codes on a reconfigurable hardware for future communications systems," *Third International Conference on 3G Mobile Communication Technologies*, Page(s):196 - 200, 2002.
- [32] T. Oenning and J. Moon, "A Low-Density Generator Matrix Interpretation of Parallel Concatenated Single Bit Parity Codes," *IEEE Trans. on Magnetics*, Vol. 37, No. 2, pp. 737-741, March 2001.
- [33] K. Sungwook, G. Sobelman, and M. Jaekyun, "Parallel VLSI architectures for a class of LDPC codes," *IEEE International Symposium on Circuits and Systems*, 2002. Volume 2, Page(s):II-93 - II-96, 2002.

## **Dr. El-Maleh's List Publications:**

- 1) **Aiman El-Maleh**, Saqib Khursheed, and Sadiq Sait, "Static Compaction Techniques for Sequential Circuits Based on Reverse Order Restoration and Test Relaxation" IEEE Transactions on Computer Aided Design of Integrated Circuits (to appear).
- 2) Sadiq M. Sait, **Aiman H. El-Maleh**, and Raslan H Al-Abaji, "Evolutionary Algorithms for VLSI Multiobjective Netlist Partitioning," Elsevier Editorial System(tm) for Engineering Applications of Artificial Intelligence (to appear).
- 3) **Aiman El-Maleh**, Saqib Khursheed, and Sadiq Sait, "Static Compaction Techniques for Sequential Circuits Based on Reverse Order Restoration and Test Relaxation" IEEE 14<sup>th</sup> Asian Test Symposium, Dec. 18-21 2005 (accepted).
- 4) **Aiman El-Maleh**, Sadiq Sait, and Syed Shazli, "Evolutionary Algorithms for State Justification in Sequential Automatic Test Pattern Generation," ENGINEERING INTELLIGENT SYSTEMS FOR ELECTRICAL ENGINEERING AND COMMUNICATIONS 13 (1): 15-21, MAR 2005.
- 5) **Aiman El-Maleh** and Yahya Osais, "A Class-based Clustering Static Compaction Technique for Combinational Circuits," The 16th International Conference on Microelectronics, 6-8 Dec. 2004, Page(s):522 – 525.
- 6) **Aiman El-Maleh** and Yahya Osais, "On Test Vector Reordering for Combinational Circuits," The 16th International Conference on Microelectronics, 6-8 Dec. 2004, Page(s): 772 - 775.
- 7) **Aiman El-Maleh** and Khaled Al-Utaibi, "An Efficient Test Relaxation Technique for Synchronous Sequential Circuits," IEEE Transactions on Computer Aided Design of Integrated Circuits, Vol. 23, No. 6, pp. 933-940, June 2004.
- 8) Aiman El-Maleh and Yahya Osais, "Test Vector Decomposition Based Static Compaction Algorithms for Combinational Circuits", **ACM Transactions on Design Automation of Electronic Systems**, Volume 8, No. 4, pp. 430-459, October 2003.
- 9) **Aiman El-Maleh**, "A Hybrid Test Compression Technique for Efficient Testing of Systems-on-a-Chip," **10th IEEE International Conference on Electronics, Circuits and Systems**, December 2003.

- 10) Yahya Osais and **Aiman El-Maleh**, "A Static Test Compaction Technique for Combinational Circuits Based on Independent Fault Clustering," **10th IEEE International Conference on Electronics, Circuits and Systems**, December 2003.
- 11) Sadiq Sait, **Aiman El-Maleh** and Raslan Al-Abaji, "Enhancing Performance of Iterative Heuristics for VLSI Netlist Partitioning", **10th IEEE International Conference on Electronics, Circuits and Systems**, December 2003.
- 12) **Aiman El-Maleh** and Khaled Al-Utaibi, "An Efficient Test Relaxation Technique for Synchronous Sequential Circuits" Proc. of the **21'th IEEE VLSI Test Symposium (VTS)**, pp. 179-185, 2003.
- 13) **Aiman El-Maleh** and Khaled Al-Utaibi, " ON EFFICIENT EXTRACTION OF PARTIALLY SPECIFIED TEST SETS FOR SYNCHRONOUS SEQUENTIAL CIRCUITS " Proc. of the **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. V-545 - V-548, 2003.
- 14) Sadiq Sait, **Aiman El-Maleh** and Raslan Al-Abaji, "SIMULATED EVOLUTION ALGORITHM FOR MULTIOBJECTIVE VLSI NETLIST BI-PARTITIONING" Proc. of the **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. V-457 - V-460, 2003.
- 15) Sadiq Sait, **Aiman El-Maleh** and Raslan Al-Abaji, "GENERAL ITERATIVE HEURISTICS FOR VLSI MULTIOBJECTIVE PARTITIONING" Proc. of the **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. V-497 - V-500, 2003.
- 16) **Aiman El-Maleh** and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational and Full-Scan Sequential Circuits" Proc. of the **20'th IEEE VLSI Test Symposium (VTS)**, pp. 53-59, 2002.
- 17) **Aiman El-Maleh** and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational Circuits Based on Critical Path Tracing" Proc. of the **9th IEEE International Conference on Electronics, Circuits and Systems**, pp. 461-465, Sep. 2002.
- 18) **Aiman El-Maleh** and Raslan Al-Abaji, "Extended Frequency-Directed Run Length Code with Improved Application to System-on-a-chip Test Data

Compression” Proc. of the 9th **IEEE International Conference on Electronics, Circuits and Systems**, pp. 449-452, Sep. 2002.

19) **Aiman El-Maleh** and Ali Al-Suwaiyan, “An Efficient Test Relaxation Technique for Combinational Logic Circuits”, Proc. of the Six’th **Saudi Engineering Conference**, Vol. 4, pp. 155-165, Dec. 2002.

20) **Aiman El-Maleh** and Raslan Al-Abaji, “On Improving the Effectiveness of System-on-a-Chip Test Data Compression based on Extended Frequency-Directed Run Length Codes” Proc. of Six’th **Saudi Engineering Conference**, Vol. 4, pp. 145-153, Dec. 2002.

21) Sadiq Sait, **Aiman El-Maleh** and Raslan Al-Abaji, “Evolutionary Heuristics for Multiobjective VLSI Nestlist Bi-Partitioning” Proc. of Six’th **Saudi Engineering Conference**, Vol. 4, pp. 131-143, Dec. 2002.

22) **AimanEl-Maleh**, Saif Al-Zahir, and Esam Khan, “A Geometric-Primitives-Based Compression Scheme for Testing Systems-on-a-Chip,” 19’th **IEEE VLSI Test Symposium (VTS)**, pp. 54-59, 2001.

23) **Aiman El-Maleh**, and Yahya Osais, “A Retiming-Based Test Pattern Generator Design for Built-In Self Test of Data Path Architectures,” **Int. Symp. on Circuits and Systems (ISCAS)**, pp. 550-553, 2001.

24) **Aiman El-Maleh**, Sadiq Sait, and Syed Shazli, “An Iterative Heuristic for State Justification in Sequential Automatic Test Pattern Generation,” 2001 **Genetic and Evolutionary Computation Conference (GECCO)**.

25) **Aiman El-Maleh**, Sadiq Sait, and Syed Shazli, “An Evolutionary Meta-Heuristic for State Justification in Sequential Automatic Test Pattern Generation,” **International Joint INNS-IEEE Conference on Neural Networks (IJCNN)**, pp. 767-772, 2001.

26) Saif Al-Zahir, **Aiman El-Maleh**, and Esam Khan, “An Efficient Test Vector Compression Technique Based on Geometric Shapes,” the 8th **IEEE International Conference on Electronics, Circuits and Systems (ICECS 2001)**, pp. 1561-1564, 2001.

27) Sadiq Sait, Habib Yousef, **Aiman El-Maleh**, and Mahmud Minhas, “Iterative

Heuristics for Multiobjective VLSI Standard Placement”, **International Joint INNS-IEEE Conference on Neural Networks (IJCNN)**, pp. 2224-2229, 2001.

28) Sadiq Sait, Habib Yousef, Junaid Khan, and **Aiman El-Maleh**, “Fuzzy Simulated Evolution for Low power and High Performance Optimization of VLSI Placement”, **International Joint INNS-IEEE Conference on Neural Networks (IJCNN)**, pp. 738-743, 2001.

29) Sadiq Sait, Habib Yousef, Junaid Khan, and **Aiman El-Maleh**, “Fuzzified Iterative Algorithms for Performance Driven Low Power VLSI Placement”, **International Conference on Computer Design (ICCD)**, pp. 484-487, 2001.

30) **Aiman El-Maleh**, Mark Kassab, and Janusz Rajski, “A Fast Sequential Learning Technique for Real Sequential Circuits with Application to Enhancing ATPG Performance,” in **Proc. of 32nd Design Automation Conference** , pp. 625-631, **June 1998**.

31) **Aiman El-Maleh**, Thomas Marchok, Janusz Rajski, and Wojciech Maly, “Behavior and Testability Preservation Under the Retiming Transformation,” **IEEE Transactions on Computer-Aided Desig, Vol. 16**, pp. 528-543, May 1997.

32) Wu-Tung Cheng, **Aiman El-Maleh**, Rob Thompson, Don Ross, and Janusz Rajski, “The Pitfalls of Necessary Assignments”, **Fourth International Test Synthesis Workshop**, May 1997, Santa Barbara, CA.

33) Thomas Marchok, **Aiman El-Maleh**, Wojciech Maly, and Janusz Rajski, “A Complexity Analysis of Sequential ATPG,” **IEEE Transactions on Computer-Aided Design.**, Vol. 15, pp. 1409-1423, Nov. 1996.

34) Janusz Rajski, **Aiman El-Maleh**, and Jerzy Tyszer, “Arithmetic BIST Tackles Embedded Cores,” **Electronic Engineering Times**, Oct. 21, 1996.

35) **Aiman El-Maleh** and Janusz Rajski, “Delay Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations,” **IEEE Transactions on Computer-Aided Design**, Vol. 14, pp. 582-590, May 1995. (A special section on 12th IEEE VLSI Test Symposium.)

36) Thomas Marchok, **Aiman El-Maleh**, Janusz Rajski, and Wojciech Maly, “Testability Implications of Performance Driven Logic Synthesis,” in **IEEE Design**

**and Test of Computers**, pp. 32-39, summer 1995.(A special issue on First International Test Synthesis Workshop.)

37) **Aiman El-Maleh**, Thomas Marchok, Janusz Rajski, and Wojciech Maly, “On Test Set Preservation of Retimed Circuits,” in Proc. of the 32nd **Design Automation Conference**, pp. 176-182, June 1995.(**Best paper award nomination.**)

38) Thomas Marchok, **Aiman El-Maleh**, Wojciech Maly, and Janusz Rajski, “Complexity of Sequential ATPG,” in Proc. of the **European Design and Test Conference**, pp. 252-261, March 1995 (**Winner of the best paper award for the most outstanding contribution in the field of test in 1995**).

39) **Aiman El-Maleh** and Janusz Rajski, “Algebraic Resubstitution with Complement and Testability Preservation,” Presented at the **First International Test Synthesis Workshop**, May 1994, Santa Barbara, CA.

40) Thomas Marchok, **Aiman El-Maleh**, Wojciech Maly, and Janusz Rajski, “Test Set Preservation under Retiming Transformation,” Presented at the **First International Test Synthesis Workshop**, May 1994, Santa Barbara, CA.

41) **Aiman El-Maleh** and Janusz Rajski, “Delay-Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations,” in Proc. of **IEEE VLSI Test Symposium**, April 1994, pp. 15-21.

42) Janusz Rajski, Jagadeesh Vasudevamurthy, and **Aiman El-Maleh**, “Recent Advances in Logic Synthesis with Testability,” in Proc. of **IEEE VLSI Test Symposium**, April 1992, pp. 254-256.

43) **Aiman H. El-Maleh**, Fayez El-Guibaly, and V.K. Bhargava, “Improving the Performance of One-Dimensional Vector Quantization Using Product Structures,” in Proc. of the 1991 **First Cyprus International Conference on Computer Applications to Engineering Systems**, Nicosia, Cyprus, July 1991, pp. 40-45.

44) **Aiman H. El-Maleh**, Fayez El-Guibaly, and V.K. Bhargava, “A Comparison of One- And Two-Dimensional Vector Quantization of Images,” in Proc. of the 1991 **IEEE Pacific Rim Conference on Communications, Computers and Signal Processing**, Victoria, Canada, Vol. 2, May 1991, pp. 490-493.

45) **Aiman H. El-Maleh** and Sadiq M. Sait, “A State Machine Synthesizer With

Weinberger Arrays,” in Proc. of the 1991 **IEEE Pacific Rim Conference on Communications, Computers and Signal Processing**, Victoria, Canada, Vol. 2, May 1991, 753-756.

46) Sadiq M. Sait and **Aiman H. El-Maleh**, “State Machine Synthesis with Weinberger Arrays,” **Int. Journal of Electronics**, Vol. 71, No. 1, pp. 1-12, July 1991.

**Patents:**

*Aiman H. El-Maleh, Wojciech Maly, Thomas E. Marchok, Janusz Rajski, “Test Pattern Generation for an Electronic Circuit Using a Transformed Circuit Description,” US Patent 5,528,604.*

## **Dr. Landolsi's Publications:**

**PhD Thesis:** "Performance of DS-CDMA Communication Systems with Generalized OQPSK Modulation," University of Michigan, USA, February 1996.

### **Journal Papers:**

1. M.A. **Landolsi**, "Performance Limits in CDMA PN Code Acquisition," under revision, *IEEE Transaction on Wireless Communications*.
2. M.A. **Landolsi**, "The Application of Low-Density Parity Check Codes to CDMA Communication over Nonlinear Bandlimited Satellite Channels," under review, *International Journal on Satellite Communication and Networking*.
3. M.A. **Landolsi**, "Minimization of Tracking Jitter in CDMA PN Code Tracking," *IEE Electronic Letters*, Vol. 40, No. 21, Oct. 2004, pp. 1352-1353.
4. M.A. **Landolsi** and W. Stark, "On The Accuracy of Gaussian Approximations in the Error Analysis of DS-CDMA Systems with OQPSK Modulation", *IEEE Trans. on Comm.*, Vol. 50, No. 12, pp. 2064-2071, December 2002.
5. M.A. **Landolsi** and W. Stark, "Effects of Filtering and Hard Limiting on the Error Performance of DS-CDMA with OQPSK-type Modulation," *IEEE Trans. on Veh. Tech.*, Vol. 51, Issue 5, September 2002, pp. 1145-1152
6. M.A. **Landolsi** and W. Stark , "DS-CDMA Chip Waveform Design for Minimal Interference under Bandwidth, Phase and Envelope Constraints," *IEEE Trans. on Comm.*, Vol. 47, No. 11, Nov. 1999.
7. M.A. **Landolsi** and W. Stark, "Optimal Chip Waveforms for DS/CDMA with Generalized Offset Quadrature Phase Shift Keying," *European Trans. on Telecommunications*, Issue 5, 1997.

### **Patents:**

1. M.A. **Landolsi**, "System and Apparatus for Designing and Producing Signaling Waveforms for DS-CDMA Communication," US Patent No. 6,570,842, May 2003.



2. A. Daraiseh, M.A. **Landolsi**, K. Basu, "Multilevel Distributed Frame Selection and Power Control CDMA Architecture with Application to Satellite Networks," US Patent No. 6,330,127, April 2002.
3. C. Yu *et al.* "Method for Optimizing Cell Site Placement," U.S Patent No. 6,094,580, July 2000.
4. Sendonaris, V. Veeravelli, M.A **Landolsi** and A. Daraiseh, "Forward Link Power Control in a Cellular Radiotelephone System," U.S Patent No. 6,085,106, July 2000.

### **Conference Papers:**

1. H.B. Ganiyu and M.A. **Landolsi**, "The Impact of Pulse Shaping on Non-coherent DLL Tracking in DS/SS Systems", accepted for publication in the 2<sup>nd</sup> Intl. Symp. Wireless Systems & Networking (ISWSN), Dhahran, KSA, Dec. 2005.
2. M.A. **Landolsi**, "Design and Performance Optimization of LDPC Codes with Short Block Length," *Proc. Intl. Conf. on Modeling, Simulation & Applied Optimization (ICSMAO)*, Sharjah, UAE, Feb. 2005.
3. B.H. Dohan and M.A. **Landolsi**, "The Impact of Fixed Point Implementation on the Performance of Semi-Random LDPC Codes," *Proc. 2<sup>nd</sup> IEEE GCC*, Bahrain, Nov. 2004.
4. M.K. Aregbesola and M.A. **Landolsi**, "A Fast Multi-Threshold Hybrid Search Scheme for CDMA PN Code Acquisition," *Proc. 2<sup>nd</sup> IEEE GCC*, Bahrain, Nov. 2004.
5. M.A. **Landolsi**, "Quadrature-spread CDMA Performance with Diversity Reception over Multipath Fading Channels," *Proc. Intl. Symp. on Wireless Syst. & Net.* ISWSN'03, March 2003, Dhahran, Saudi Arabia.
6. M.A. **Landolsi**, "On the Accuracy of Gaussian Approximations in the Error Analysis of CDMA with OQPSK Spreading," *Proc. 14<sup>th</sup> Intl. Conf. Wireless Comm.* WIRELESS'02, July 2002, Calgary, Canada.
7. Y. Mao, A. Banihashemi and M. **Landolsi**, "Performance and Complexity Comparison of Short LDPC Codes and Turbo Product Codes," *Proc. IEEE Wireless Comm. & Net. Conf.* WCNC, September 2000. Chicago, IL, USA.
8. M. El-Tarhuni and M. **Landolsi**, "The Effect of Chip Waveform Shaping on the Synchronization Performance of DS-CDMA Signals," *Proc. IEEE*

VTC'99, TX, USA.

9. A. Daraiseh and M. **Landolsi**, "Optimized Forward Link Power Allocation for Mobiles in Soft Handoff", *Proceedings of the IEEE VTC'98*, Ottawa, Canada.
10. G. Wan, M. **Landolsi** and S. Tseng, "Performance Analysis of the Forward and Reverse Control Channels in CDMA Wireless Networks," *Proc. IEEE VTC'98*, Ottawa, Canada.
11. M.A. **Landolsi**, V. Veeravelli, and N. Jain, "New Results on the Reverse Link Capacity of CDMA Cellular Networks," *Proc. IEEE VTC'96*, Atlanta, GA, USA.
12. M.A. **Landolsi** and W. Stark, "DS/CDMA Chip Waveform Design for Optimal Power-Bandwidth Performance", *Proc. IEEE PIMRC'95*, Toronto, ON, Canada.
13. M.A. **Landolsi** and W. Stark, "Performance of DS/CDMA Communication Systems with Continuous Phase Modulation", *Proc. IEEE MILCOM'93*, Boston, MA.