Test Data Volume Reduction of Scan-Based Deterministic Test based on Scan Chains Compatibility using Partitioning & Relaxation

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by

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Contents

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Abstract

As IC design has entered into the nanometer scale integration, the design test complexity has increased tremendously because of the extent of sophistication possible at this integration level. Scan-based design test strategy is the most widely used solution to achieve the high level of fault coverage desired for such complex designs, and especially for the SoC based design paradigm. However, test data volume, test application time and power consumption have increased proportionately with integration scale and so has, ultimately, the cost of test. Scan-based test alone does not offer much for these problems. Test data compression techniques have been increasingly used recently to cope with this problem. This work proposes a test data compression technique for multiple scan designs that aims to improve upon the existing techniques by taking advantage of some novel observations. We propose the use of test data partitioning and relaxation-based decomposition of certain bottleneck vectors to achieve user specified compression ratios with an associated decompression hardware in an optimal manner.

1 Introduction

Increasing test cost is a major challenge facing the IC design industry today [1]. Shrinking process technologies and increasing design sizes have led to highly complex, billion-transistor integrated circuits. Testing these complex

ICs to weed out defective parts has become a major challenge. To reduce design and manufacturing costs, testing must be quick and effective. The time it takes to test an IC depends on test data volume. The rapidly increasing number of transistors and their limited accessibility has spurred enormous growth in test data volume. Techniques that decrease test data volume and test time are necessary to increase production capacity and reduce test cost.

The latest system-on-a-chip (SoC) designs integrate multiple ICs (microprocessors, memories, DSPs, and I/O controllers) on a single piece of silicon. SOCs consist of several reusable embedded intellectual-property (IP) cores provided by third-party vendors and stitched into designs by system integrators. Testing all these circuits when they are embedded in a single device is far more difficult than testing them separately. The testing time is determined by several factors, including the test data volume, the time required to transfer test data to the cores, the rate at which the test patterns are transferred (measured by the test data bandwidth and the ATE channel capacity), and the maximum scan chain length. For a given ATE channel capacity and test data bandwidth, reduction in test time can be achieved by reducing the test data volume and by redesigning the scan chains. While test data volume reduction techniques can be applied to both soft and hard cores, scan chains cannot be modified in hard (IP) cores.

Test patterns are usually generated and stored on workstations or high-performance personal computers. The increased variety of ASICs and decreased production volume of individual types of ASICs require more frequent downloads of test data from workstations to ATE. In addition, because of the sheer size of test sets for ASICs, often as large as several gigabytes, the time spent to download test data from computers to ATE is significant. The download from a workstation storing a test set to the user interface workstation attached to an ATE is often accomplished through a network. The download takes several tens of minutes to hours [12]. The test set is then transferred from the user interface workstation of an ATE to the main pattern memory through a dedicated high speed bus. The latter transfer usually takes several minutes. The transfer of data from a workstation to an ATE is shown in Figure 1.

During the download period of a test set, the ATE is idle, wasting this valuable resource. The overall throughput of an ATE is affected by the download time of test data and the throughput becomes more sensitive to the download time with the increased variety of ASICs. One common approach to improve the throughput of an ATE is to download the test data of the

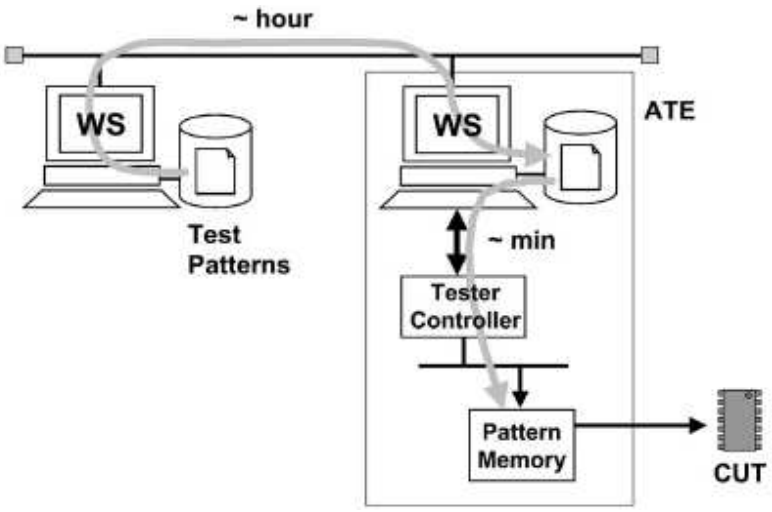

Figure 1: Download of test data to ATE [7]

next chip during the testing of a chip. This cuts down the effective download time of test data, but the approach alone may not be sufficient. An ATE may finish testing of the current chip before the download of the next test data is completed.

ATE costs have been rising steeply. Achieving satisfactory SOC test quality at an acceptable cost and with minimal effect on the production schedule is also becoming increasingly difficult. High transistor counts and aggressive clock frequencies require expensive automatic test equipment (ATE). More important, they introduce many problems into test development and manufacturing test that decrease product quality and increase cost and time to market. A tester that can accurately test todays complex ICs costs several million dollars. According to the 1999 International Technology Roadmap for Semiconductors [2], the cost of a high-speed tester will exceed $20 million by 2010, and the cost of testing an IC with conventional methods will exceed fabrication cost.The increasing ratio of internal node count to external pin count makes most chip nodes inaccessible from system I/O pins, so controlling and observing these nodes and exercising the numerous internal states in the circuit under test is difficult. ATE I/O channel capacity, speed, accuracy, and data memory are limited. Therefore, design and test engineers need new techniques for decreasing data volume.

Scan-based test has become the method of choice in face of increasing design complexity [8] as it offers the highest levels of fault coverage conveniently

by using electronic design automation (EDA) tools compared to alternatives such as non-scan, partial scan and Built-In-Self-Test (BIST). Built-in self-test (BIST) has emerged as an alternative to ATE-based external testing [3]. BIST offers a number of key advantages. It allows precomputed test sets to be embedded in the test sequences generated by on-chip hardware, supports test reuse and at-speed testing, and protects intellectual property. While BIST is now extensively used for memory testing, it is not as common for logic testing. This is particularly the case for nonscan and partial-scan designs in which test vectors cannot be reordered and application of pseudorandom vectors can lead to serious bus contention problems during test application. Moreover, BIST can be applied to SOC designs only if the IP cores in it are BIST-ready. Since most currently available IP cores are not BIST-ready, BIST insertion in SOCs containing these circuits is expensive and requires considerable redesign.

As chip designs become larger and new process technologies require more complex failure modes, the length of scan chains and the number of scan patterns required have increased dramatically. To maintain adequate fault coverage, test application time and test data volume have also escalated, which has driven up the cost of test. Scan chain values currently dominate the total stimulus and observe values of the test patterns, which constitute the test data volume. With the limited availability of inputs and outputs as terminals for scan chains, the number of flip-flops per scan chain has increased dramatically. As a result, the time required to operate the scan chains, or the test application time, has increased to the extent that it is becoming uneconomic to employ scan test on complex designs. To understand the impact of shift time on test application time, consider the typical sequence involved in processing a single scan test pattern shown in Figure 2. All these steps - excluding the shift operations in steps 2 and 7 - require one clock period on the tester. The shift operations, however, take as many clock periods as required by the longest scan chain. Optimizations (such as overlapping of scan operations of adjacent test patterns) still do not adequately influence the unwieldy test application time required by the scan operation. For a scan-based test, test data volume can be approximately expressed as

$$Test\ data\ volume \approx scan\ cells \times scan\ patterns$$

Assuming balanced scan chains, the relationship between test time and test data volume is then

$$Test\ time \approx \frac{scan\ cells \times scan\ patterns}{scan\ chains \times frequency}$$

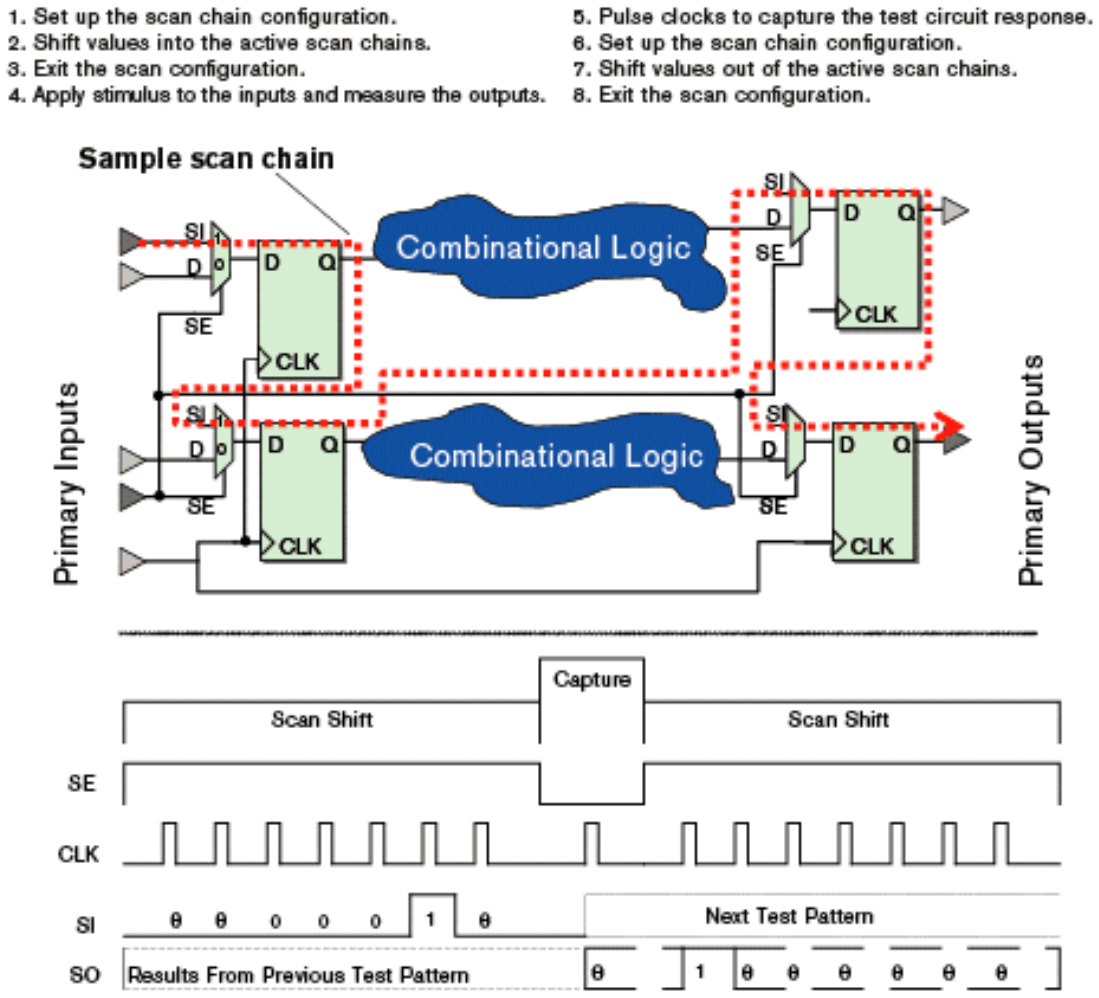

Figure 2: Steps in a scan-based testing [5]

Consider an example circuit consisting of 10 million gates and 16 scan chains. Typically, the number of scan cells is proportional to the design size. Thus, assuming one scan cell per 20 gates, the total test time to apply 10,000 scan patterns at a 20-MHz scan shift frequency will be roughly 312 million test cycles or equivalently 15.6 seconds. As designs grow larger, maintaining high test coverage becomes increasingly expensive because the test equipment must store a prohibitively large volume of test data and the test application time increases. Moreover, a very high and continually increasing logic-to-pin ratio creates a test data transfer bottleneck at the chip pins. Accordingly, the overall efficiency of any test scheme strongly depends on the method employed to reduce the amount of test data.

Test resource partitioning (TRP) offers a promising solution to these problems by moving some test resources from ATE to chip [4]. One of possible TRP approach is based on the use of test data compression and on-chip decompression, hence reducing test data volume, decreasing testing time, and allowing the use of slower testers without decreasing test quality. Test-data compression offers a promising solution to the problem of reducing the test-data volume for SoCs, especially if the IP cores in the system are not BIST-ready. In one approach, a precomputed test set T_D for an IP core is compressed (encoded) to a much smaller test set T_E, which is stored in ATE memory. An on-chip decoder is used for pattern decompression to obtain T_D from T_E during test application (See Figure 3). Another approach is to introduce logic in the scan path at scan-in and scan-out. Test data volume and test application time benefits are achieved by converting data from a small scan interface at the design boundary to a wide scan interface within the design. This approach enables significantly more scan chains in the design than allowed by its signal interface [5].

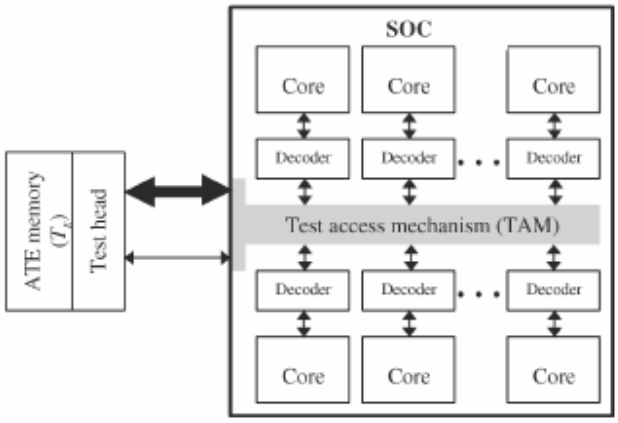

Figure 3: Conceptual architecture for testing an SoC by storing the encoded test data T_E in ATE memory and decoding it using on-chip decoders.[4]

A majority of bits in test patterns are unspecified. Prior to the rise of test data volume and test application time, the typical industry practice was to randomly fill the unspecified bits [6]. Test compression technology creatively discovers alternatives for handling these randomly filled bits, which decreases test data volume and test application time efficiency.

Because the goal of test compression is to increase the efficiency of scan test-

ing, this new technology provides better results without losing the existing benefits of scan. However, not every test compression technique is compatible with scan technology.

Simplicity is a very important feature of scan technology. Scan test is easy to understand, implement, and use. Because of this simplicity, scan has been incorporated successfully in design flows without disrupting important layout and timing convergence considerations. Even more importantly, the following features of scan test are now widely understood in the industry [5]:

- Scan has "low" area overhead. Scan has proven to be a critical design function. Its area requirements are accepted and are no longer considered to be an overhead.
- As a result of implementing scan chains, scan adds only combinational logic to the existing edge-triggered flip-flops in the design.
- Scan does not require changes to the netlist for blocking Xs in the design. An unknown circuit response during test does not inhibit the application of the test itself.
- Scan has led to the development of several useful scan diagnostic solutions that rely on statistical analysis methods, such as counting the number of fails on the tester on various scan elements.

In the next section, we present a literature review of existing techniques for test data volume reduction, which is followed by a description of our proposed technique.

2 Literature Review

The problem of increasing test data volume has been addressed through a variety of approaches. In this section we briefly review these approaches for scan-based deterministic test. Previous work in this area can be broadly categorized as follows:

- Compression techniques that use some form of coding, such as run-length encodings, Huffman encodings, statistical encodings etc. which are often borrowed from existing data compression methods and modified to suit the requirements of test data compression. Dictionary based compression can also be included under this category.

- Techniques that rely on properties of LFSRs to encode the test sets to reduce the scan input data
- Multiple scan chain designs that use a single scan input to broadcast to multiple internal scan chains.
- Compatibility-based reduction of multiple scan-chains in which a smaller number of external scan chain drive a larger number of internal scan chains with a decoder at the interface.

Other techniques have also been reported which do not fall under the above mentioned broad categories. Multiple scan chain structures have also been reported which can work along with the second and third approach. Also, the techniques can be categorized into ones that do not require any modification to ATPG process and work with an existing test set and those that necessitate modification to the ATPG process.

Data compression techniques in the first category are used to compress the precomputed test-data set T_D, often provided by core vendor, to a smaller test set T_E which is then stored in the ATE's memory. An on-chip decoder decompresses T_E to T_D to be applied to the system under test. Most compression techniques of this type compress T_D without requiring any structural information about the embedded cores. Proposed compression schemes include statistical coding [13, 14], selective Huffman coding [15], mixed run-length and Huffman coding [16], Golomb coding [17], frequency-directed run-length (FDR) coding [18], geometric shape-based encoding [19], alternating run-length coding using FDR [20], extended FDR coding [21], MTC coding [22], and variable-input Huffman coding (VIHC) coding[23], nine-coded compression technique [24], Burrows-Wheeler transform based compression [7], and arithmetic coding [25]. Several dictionary-based compression methods have been proposed to reduce test-data volume. In [14], frequently occurring blocks are encoded into variable-length indices using Huffman coding. A dictionary with fixed-length indices is used to generate all distinct output vectors in [26]. Test-data compression techniques based on LZ77 and LZW and test-data realignment methods are proposed in [27, 29, 28], respectively. The method proposed in [30] is a compression technique using dictionary with fixed-length indices for multiple-scan chain designs. A hybrid coding strategy, combining alternating run-length and dictionary-based encoding, is also proposed [31] to improve the compression.

The next class is using LFSR reseeding[32, 33, 34, 35, 36, 37]. The original test compression methodology using LFSR reseeding was proposed in [32].

A seed is loaded into an LFSR and then the LFSR is run in an autonomous mode to fill a set of scan chains with a deterministic test pattern. If the maximum length of each scan chain is L, then the LFSR is run for L cycles to fill the scan chains. Different seeds generate different test patterns, and for a given set of deterministic test cubes (test patterns where bits unassigned by ATPG are left as dont cares), the corresponding seeds can be computed for each test cube by solving a system of linear equations based on the feedback polynomial of the LFSR. The Embedded Deterministic Test method described in [39] uses a ring generator which is an alternative linear finite state machine that offers some advantages over an LFSR.

Methods that reduce test volume and time using design modification include the proposed Illinois scan architecture (ILS) [40], which needs fault simulation and test generation as postprocessing steps to get high fault coverage. Illinois Scan Architecture (ISA) reduces data volume and test application time by splitting the scan chain into multiple segments and broadcasting the data to all of them as long as the segments data are compatible. The basic architecture for Illinois scan is can be found in [41]. A given scan chain is split into multiple segments. Since a majority of the bits in ATPG patterns are don't care bits, there are chances that these segments will have compatible vectors (not having opposite care bits in one location). In this case, all segments of a given chain are configured in broadcast mode to read the same vector. This speeds up the test vector loading time and reduces the data volume by a factor equivalent to the number of segments. In case if the segments within a given scan chain are incompatible, the test vector needs to be loaded serially by reconfiguring the segments into a single long scan chain. The fact that a majority of the ATPG bits (95-99% [6]) are don't care bits makes ISA an attractive solution for data volume and test time. Several enhancements to the scan architecture have been proposed and discussed in the literature for multiple reasons. Lee et. al. presented a broadcasting scheme where ATPG patterns are broadcasted to multiple scan chains within a core or across multiple cores. The broadcast mode is used when the vectors going into multiple chains are compatible [42]. [43] introduced a token scan architecture to gate the clock to different scan segments while taking advantage of the regularity and periodicity of scan chains. Another scheme for selective triggering of scan segments was proposed in [48]. A novel scheme was presented in [47] to reduce test power consumption by freezing scan segments that don't have care bits in the next test stimulus. By only loading the segments that have care bits, data volume, application time, and test power consumption are all reduced at once. Only one segment of the scan chain is controlled an observed at a time. A reconfigurable scheme was

introduced in [44] to use mapping logic to control the connection of multiple scan chains. This increases the chances of compatibility between multiple chains and hence makes room for additional compaction. A new scan architecture was proposed in [46] to order the scan cells and connect them based on their functional interaction. A circular scan scheme was presented in [45] to reduce test data volume. A segmented addressable scan architecture [49] has also recently been proposed.

The idea of input compatibility was first introduced in context of width compression for BIST based test generation process in [50]. Width reduction for BIST has been achieved by merging directly and inversely compatible inputs [50], by merging decoder(d)-compatible inputs [51], and, finally, by merging combinational(C)-compatible inputs [10]. While d-compatible inputs require that no more than a single "1" be present at any of the test vectors, C-compatibility necessitates that an input can be driven by a combinational function of other inputs. While increasing the number of compatibility classes increases the efficiency of width compression, identification of such compatibility classes increases the complexity of the algorithm significantly. The idea of compatibility for reducing scan test data has been applied in [52].

The next section presents our proposed test data compression scheme.

3 Proposed Test Data Compression Technique for Multiple Scan-Chains Input

In this work we propose a scan test data compression technique that works with a multiple scan chains input test access mechanism [9]. The technique extends the idea of scan chains compatibility [10] and tries to overcome the bottlenecks that prevent greater achievable compression. The main contributions of the proposed technique are:

1. It uses an approach for optimally partitioning the test data into groups of scan chains that are maximally compatible among themselves, thus resulting in fewer scan chains required to compress that group

2. Those scan vectors (labeled as bottleneck vectors) that limit achieving a desired compression level are treated with an efficient relaxation-based test vector decomposition technique[11] in an intelligent manner so as to increase the unspecified bits, resulting in better compression of the resulting relaxed vectors.

Hence, the goal of the proposed technique is to achieve the user specified compression level by using test set partitioning, and, relaxation-based decomposition of bottleneck vectors, if there exists such a solution for the given test data set.

To understand how the proposed technique improves compression, consider the following properties of scan test data vectors and scan chains compatibility:

- Given a number of parallel scan chains, the compatibility analysis gives a reduced number of *representative* parallel scan chains if the given parallel chains are compatible amongst themselves.
- The extent of compatibility achieved depends upon how many bits are specified per scan vector. The lesser the specified bits, the lesser the conflicts, resulting in greater compatibility between the set of parallel chains.
- An input scan vector can be decomposed into multiple scan vectors each having greater unspecified bits than the original vector but each vector will now cover less faults than the original more specified vector.
- Some vectors in the relaxed test set can be omitted if the they cover faults that are all covered by other vectors, to avoid unnecessary increase in the size of test set.
- The compatibility analysis can be applied to parallel scan chains of a single vector or a set of vectors. The amount of conflict tends to increase the longer the chains are (because of the extent of specified bits present).
- Compatibility analysis per vector thus gives the lower bound on achievable *representative* parallel scan chains for a given test set for a specified number of parallel scan chains per vector.

In the next two sections we explain in detail how these properties are utilized by using test data partitioning along with relaxation-based test vector decomposition in the proposed technique.

3.1 Partitioning Test Set into Groups of Maximally Compatible Scan Vectors

The algorithm comprises of the following steps:

1. The scan vectors in the given test set are configured into a specified number of parallel scan chains.

2. The desired level of compression is used to calculate the maximum number of *representative* parallel scan chains that are acceptable, called hereafter as a *threshold*.

3. The compatibility analysis is applied separately to each individual scan vector in the test set. This gives the *representative* number of parallel scan chains per vector, called hereafter as the *representative count*.

4. Those vector whose *representative count* exceeds the *threshold* after the analysis in Step 3 are separated into a set called *'bottleneck vectors'*.

5. The remaining set of vectors, hereafter called as *acceptable vectors*, are sorted based on their *representative count* in a descending order.

6. The first vector in the sorted list forms the first (default) partition.

7. The next vector is analyzed for compatibility with existing partition(s) starting at the top of available partitions list. If it is found to be compatible with the tested partition while satisfying the *threshold*, it is included in that partition. Otherwise, another available partition is considered to be checked with this vector.

8. If the list of available partitions has been exhausted and still the condition in Step 7 is not satisfied, a new partition is created with the current vector.

9. The steps 7-8 are repeated until all vectors in the sorted*acceptable vectors* list have been processed.

10. The resulting configuration of partitions achieves the desired compression ratio excluding *bottleneck vectors*.

To understand the working of above algorithm, we consider a simple example. The example shows the potential benefits of partitioning and how the bottleneck vectors are identified. Consider a test set with only three vectors where each vector is configured into four scan-chains of length three as shown in Figure 4. Let the targeted compression be 50%. We first consider the complete test set and find compatibility among the parallel scan chains. Figure 5 shows the resulting compatibility graph which indicates no compatibility between parallel chains and hence there is no compression. Next we consider each vector separately and construct the individual compatibility graphs for

Vector	SC_1	SC_2	SC_3	SC_4
1	0 X X	X 1 0	1 1 X	X 1 1
2	0 X 1	1 X 0	X 0 1	X 1 0
3	0 0 0	1 X 0	X 1 1	X 0 1

Figure 4: Example test set to illustrate the algorithm

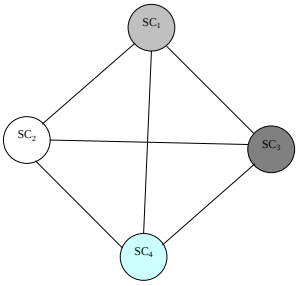

Figure 5: Conflict graph for the complete test set

each as shown in Figures 6,7,8. It can be seen that both the first and second vector satisfy the *threshold* individually while the third vector achieves no reduction. Also, it is clear that vectors 1 and 2 cannot be combined in a single partition that will satisfy the *threshold* and hence two partitions are created each with vectors 1 and 2 respectively. In this way we have partitioned the test set to satisfy the *threshold* but we still have a third vector that exceeds *threshold*. This is identified as the *bottleneck* vector which will be dealt with as explained in Section 3.2.

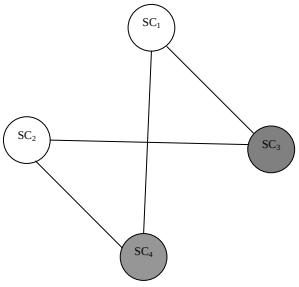

Figure 6: Conflict graph for vector 1

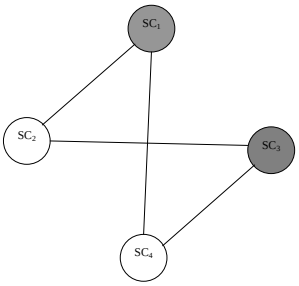

Figure 7: Conflict graph for vector 2

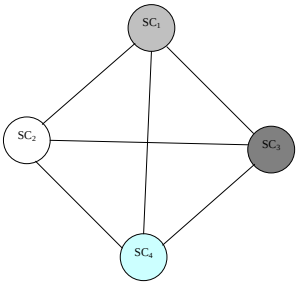

Figure 8: Conflict graph for vector 3

It should be mentioned here that the heuristic mentioned in steps 5-9 does not necessarily give the minimal number of partitions and is by no means the only method that can be used. Other methods will be explored in course of this work. The need to optimize the number of partitions is to minimize the resulting decompression hardware overhead, as detailed in Section 3.3. In the next section, we explain how relaxation-based decomposition is applied on *bottleneck vectors* to ultimately achieve the desired compression ratio.

3.2 Selective Relaxation-Based Decomposition of Test Vectors

To achieve the desired compression ratio, the *bottleneck vectors* can be decomposed until the resulting vectors satisfy the *threshold*. *Bottleneck vectors* are decomposed based on the relaxation technique proposed in [11]. The relaxed vectors are then made members of existing partitions (or new partitions) and redundant vectors are dropped accordingly. The goal at this stage is to minimize the number of vectors resulting from relaxation-based decomposition to just the required level while also minimizing the existing partitions. To achieve this, an efficient approach might be first fault simu-

Vector	SC_1	SC_2	SC_3	SC_4
3	0 0 0	1 X 0	X 1 1	X 0 1
3a	0 X 0	X X 0	X 1 1	X X 1
3b	X 0 X	1 X X	X X 1	X 0 1

Figure 9: Decomposition of vector 3 into two vectors 3a and 3b

late the more specified representative vectors in all partitions to find out all faults detected by the set of *acceptable vectors*. The set of remaining faults can then be used to incrementally decompose the *bottleneck vectors* to target only those faults that are present in remaining faults list. This decomposition is carried on to a point where the decomposed vectors satisfy the *threshold*.

Consider the *bottleneck vector* identified in the earlier example. Suppose that this vector is decomposed into two vectors 3a and 3b as shown in Figure 9, each detecting only a subset of faults detected by the original vector. The compatibility graphs of these vectors are shown in Figures 10,11. The decomposed vectors satisfy the *threshold*. Now these decomposed vectors can be merged with the existing partitions or new partitions can be created if required.

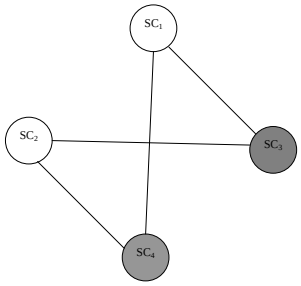

Figure 10: Conflict graph for vector 3a

In the next section, we mention the decompression hardware requirements.

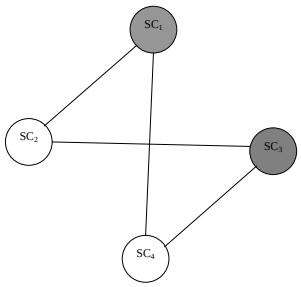

Figure 11: Conflict graph for vector 3b

3.3 Decompression Hardware

The decompression hardware builds upon the structure of compatibility based decompression structures [10] with addition of MUXes at the inputs to account for different partitions' configuration. The size of MUXes required depends upon the number of partitions to be accommodated as this determines the number of inputs of the MUXes. No MUXes are required for a single partition and therefore, the number of partitions determine the area overhead of decompression structure and thus the need to optimize the number of partitions. It should be noted that a tradeoff exists between the desired compression ratio and, (i) the decompression hardware size (number of partitions), (ii) the *bottleneck vectors* count and thus an increase in the number of vectors existing after relaxation based decomposition. Although the test vector increase affects compression ratio, the increased compatibility can counter that increase. However, the test application time is also affected and so this step has to be applied in an intelligent manner to achieve the best tradeoff.

4 Project Objectives

The principle objectives of this project are as follows:

1. Developing an efficient partitioning algorithm for the test vectors with the target of minimizing the number of partitions under a given compatibility constraint.

2. Developing an efficient relaxation-based test vector decomposition algorithm based on which the uncompressable bottleneck vectors are decomposed to trade off the increase in number of patterns and in compatibility.

3. Designing a reconfigurable broadcast combinational network for configuring the scan chains into several compatibility classes.

4. Automating the design and synthesis of the reconfigurable broadcast network.

5. Applying the algorithms to benchmark circuits.

6. Publishing the work in a refereed conference and journal.

TASK	MONTH								
	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18
1. Development of a graph-coloring based compatibility analysis technique.	↔								
2. Development of an efficient partitioning technique minimizing the number of partitions under a given compatibility constraint		↔	↔	↔					
3. Development of an efficient relaxation-based test vector decomposition technique.				↔	↔	↔			
4. Performing Experiments on benchmark circuits.				↔		↔		↔	
5. Designing a reconfigurable broadcast combinational network for configuring the scan chains into several compatibility classes.							↔		
6. Automating the design and synthesis of the reconfigurable broadcast network.							↔	↔	
7. Progress reports.			↔			↔			
8. Preparing final report and publications.									↔

Figure 12: Work Plan Time Table

5 Statement of Work & Schedule

The time span of this project is eighteen (18) months during which eight tasks will be carried out. Figure 12 shows a schedule of these tasks indicating the time requirement of each. The investigators will be involved in all the stages of the project and will work for the whole duration of the project. A graduate student will also assist during the entire duration of the project. The investigators will hold meetings as often as necessary (minimum once a week) to coordinate their work and to make necessary decisions. Periodic progress reports will be submitted every 6 months summarizing the status and accomplishments of the project and a final report documenting the project achievement will be submitted at the end of the project. The graduate student will be involved in the project development and the implementation of the proposed algorithms, and in running experiments on benchmark circuits.

5.1 Monitoring and Evaluation Plan

The project team consists of a principal investigator, co-investigator, and one graduate student. Responsibilities will be divided among the two senior investigators on the basis of their previous experience and background.

Dr. Aiman El-Maleh holds a B.Sc. in Computer Engineering, with first honors, from King Fahd University of Petroleum & Minerals in 1989, a M.A.SC. in Electrical Engineering from University of Victoria, Canada, in 1991, and a Ph.D in Electrical Engineering, with deans honor list, from McGill University, Canada, in 1995. Dr. El-Maleh is an Assistant Professor in the Computer Engineering Department at King Fahd University of Petroleum & Minerals since September 1998. He was a member of scientific staff with Mentor Graphics Corp., a leader in design automation, from 1995-1998. His research interests are in the areas of synthesis, testing, and verification of digital systems. In addition, his research interests include VLSI design, design automation, and computer arithmetic. He won the best paper award for the most outstanding contribution in the field of test for 1995 at the European Design & Test Conference. His paper, presented at the 1995 Design Automation Conference, was also nominated for best paper award. He also holds one US patent. Dr. El-Maleh was a member of the program committee of the Design Automation and Test in Europe Conference (DATE98).

Ahmad Al-Yamani is an assistant professor in the computer engineering department at King Fahd University of Petroleum and Minerals and a consulting assistant professor in the electrical engineering department at Stanford

University. He received a PhD in Electrical Engineering and an MSc in Management Science and Engineering from Stanford. Before that, he received an MSc and a BSc in Computer Engineering from KFUPM. In 2002 he was appointed as the assistant director of Stanford Center for Reliable Computing. Ahmad serves as an adjunct faculty at Santa Clara University. He also had some industrial experience in VLSI design and test with the advanced development labs of LSI Logic and in computer networks performance analysis with AMD.

6 Utility Value

The utility value of this project is many-fold, namely:

1. The results of this research can be used by chip manufacturing and testing industry to reduce the cost of testing in the overall chip production cost.

2. The results of this work can be used by other investigators in academia and industry to enhance existing methods.

3. The project provides an opportunity for training of graduate students on conducting scientific research.

7 Detailed Budget

7.1 Investigators

Both the principle investigator and co-investigator for 18 months during the regular semesters for the entire duration of the project. They will receive payments as per the university regulations. The graduate student(s) will assist in the implementation aspects of the research. His total compensation will be (10,800/- per Graduate Student/Research Assistant).

Dr. Aiman El-Maleh (PI)	SR 1,200 X 18 = SR 21,600
Dr. Ahmad Al-Yamani (CO-I)	SR 1,000 X 18 = SR 18,000
Graduate Student	SR 600 X 18 = SR 10,800
Subtotal	SR 50,400

7.2 Equipment, Materials and Charges

Facilities available at KFUPM will be used at no charge to the project. Additional equipment required for the project includes an HP laser printer with an estimated amount of SR 1500/-. Stationary and miscellaneous expenses for consumables such as floppies, CDs, paper, printer toner, etc., will amount to SR 2,000/-, purchase of literature and books, etc., will require SR 2,500/-. A secretary will work for the entire duration of the project. SR 2,000/- for payments to secretary will be required.

Individual items of the budget are summarized below:

Man Power	SR 50,400/-
Laser Printer	SR 1,500/-
Books, other literature	SR 2,500/-
Stationary and Miscellaneous	SR 2,000/-
Secretary	SR 2,000/-
Conference Attendance (1 Trip)	SR 10,000/-
The total cost[1] of the project is estimated to be	SR 68,400/-

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Dr. Ahmad Al-Yamani

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