

# Transistor-Level Defect Tolerant Digital System Design at the Nanoscale

Research Proposal Submitted to  
Internal Track  
Research Grant Programs

By

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## Abstract

Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits beyond the scaling limits reached by CMOS technology. Industrial research is indicating that nanodevices-based circuit design will be based on the acceptance that a certain percentage of devices in the design will be defective. In this work, we investigate a defect-tolerant technique that adds redundancy at the transistor level and provides built-in immunity to permanent defects. The investigated technique is based on replacing each transistor by an  $N^2$ -transistor structure ( $N=2, 3, \dots, k$ ). An  $N^2$ -transistor structure guarantees defect tolerance of all defects of multiplicity  $\leq (N-1)$  in each transistor structure. Thus, a large number of multiple defects, distributed among the structures, can be tolerated. In addition, interconnect defects can be equally tolerated. Our initial results on the tolerance of stuck-open and stuck-short defects based on the quadded-transistor structure ( $N=2$ ) are promising. Further analysis and extension of the technique for tolerance of bridging faults is required to demonstrate the applicability of the technique to practical designs. Extension of the technique to handle soft errors will also be proposed. An important advantage of the proposed transistor-level defect tolerant technique is that it fits well in existing design and test methodologies. Comparison of defect tolerance of this approach against other recently proposed defect-tolerant approaches will be evaluated experimentally. Furthermore, comparison of defect tolerance between circuits implemented based on the quadded-transistor structure and those implemented based on transistors with quadruple the feature sizes will be conducted based on inductive fault analysis. We predict that the combination of defect tolerance at both the transistor level and gate level will result in a significant improvement in circuit defect tolerance. For example, implementing majority gates with the  $N^2$ -transistor structure in Triple Modular Redundancy defect-tolerant techniques is considered promising and will be investigated in this work. Finally, the application of the quadded-transistor structure in the defect tolerance of logic implemented based on crossbar switches and FPGAs will be investigated. The regularity in crossbar switches and FPGAs make them excellent candidates for implementations based on nanotechnology. This will be evaluated and compared against recently proposed defect avoidance techniques.

## 1. Introduction

With CMOS technology reaching the scaling limits, the need for alternative technologies became necessary. Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits the next step. It is estimated that molecular electronics can achieve very high densities ( $10^{12}$  devices per  $\text{cm}^2$ ) and operate at very high frequencies (of the order of THz) [1]. Several successful nano-scale electronic devices have been demonstrated by researchers, some of the most promising being carbon nanotubes (CNT) [2], silicon nano-wires (NW) [3,4], and quantum dot cells [5]. It has been shown that using self-assembly techniques, we can overcome the limitations posed by lithography for the smallest feature size [1]. Currently, due to fabrication regularity imposed by the self assembly process, only regular structures can be built. Hewlett-Packard has recently fabricated 8 X 8 crossbar switches using molecular switches at the crosspoints [6]. They observed that only 85% of the switches were programmable while the other 15% were defective.

Whether nanotechnology circuits are implemented using self assembly or lithography processes, defect rates are rising substantially. At these nanometer scales, the small cross section areas of wires make them fragile, increasing the likelihood that they will break during assembly. Moreover, the contact area between nanowires and between nanowires and devices depends on a few atomic-scale bonds resulting in some connections being poor and effectively unusable [4, 6, 7]. With such high defect rates, defect-tolerant methods have to be devised for the emerging nanotechnology devices. Discarding all parts with any defects in them is not affordable any more as the yield hit will be substantial. Therefore, the necessity to cope with intrinsic defects at the circuit level must be recognized as a key aspect of nanodevices-based designs. To

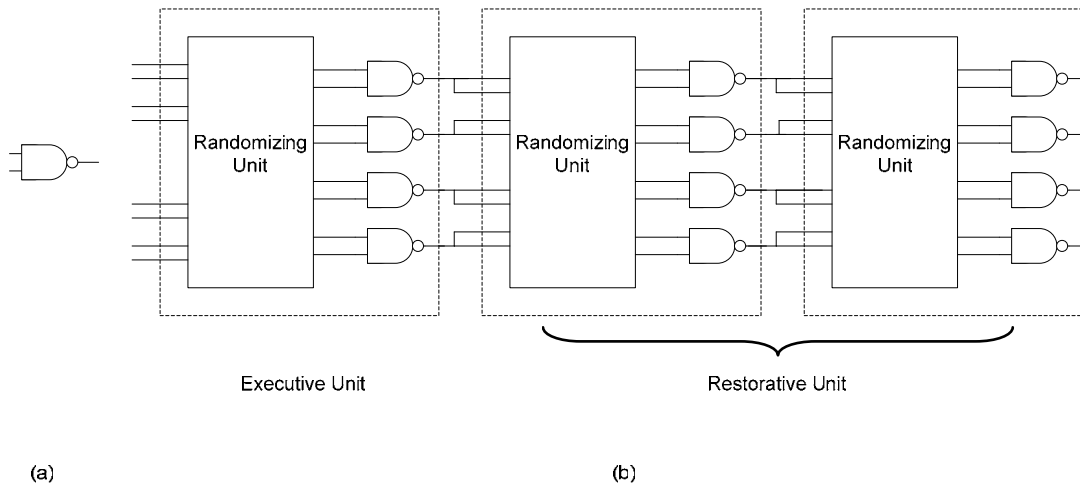
implement such robustness and defect tolerance, circuit design techniques capable of absorbing a number of defects and still be able to perform their functions need to be investigated.

Typical approaches to reliable system design include defect-tolerant and defect avoidance techniques [8]. Defect-tolerant techniques are based on adding redundancy in the design to tolerate defects or faults. However, defect avoidance techniques are based on identifying defects and bypassing them based on reconfiguration. Examples of defect-tolerant techniques are the multiplexed logic approach [9], N-tuple modular redundancy (NMR), Triple-modular redundancy (TMR) and Triple Interwoven Redundant logic (TIR) [10, 11], cascaded triple modular redundancy (CTMR) or recursive triple modular redundancy (RTMR) [12, 13], and quadded logic (QL) [10, 11, 14, 15]. Examples of the defect-avoidance techniques are [7, 8, 16-19].

While both approaches address the defect-tolerance issue, it is unclear from the literature which approach is more effective since the effectiveness of defect-tolerant approaches based on classical techniques such as TMR, is limited by the arbitration unit, whilst defect avoidance techniques require extensive defect mapping and reconfiguration infrastructure.

To tolerate defects, redundancy can be added at the transistor level, gate level or functional block level. In this work, we evaluate defect tolerance based on redundancy addition at the transistor level. We compare this approach with recent defect-tolerant techniques based on adding redundancy at the gate level. The comparison will be made through analysis of the most occurring defects including transistor stuck-open, transistor stuck-short and bridging faults.

We believe that defect tolerance to be effective needs to be addressed at different levels including transistor-level, gate-level and functional-block level. In this work, we



**Figure 1 (a) Original 2-input NAND gate, (b) von Neumann's multiplexed logic for the 2-input NAND gate with N=4.**

will evaluate the combination of defect-tolerant techniques at the gate and transistor-level.

Crossbar switches are considered the basic building blocks in recently proposed nano architectures. Defect tolerance of logic implemented based on the quadded transistor structure in crossbar switches will be investigated and compared with other defect avoidance techniques. The regularity of FPGAs makes them suitable candidates for nanotechnology implementation. In this project, we plan to investigate defect tolerance options for FPGA circuits as a case study.

## 2. LITERATURE SURVEY

### 2.1 Defect-Tolerant Techniques

The multiplexed logic approach, motivated by the pioneering work of John von Neumann [9], began as an attempt to build early digital computers out of unreliable components. This approach and subsequent derivatives [10, 14-15] have provided insight on how to design reliable nanoelectronic systems out of components that

might fundamentally be less reliable than those of currently available technologies. In the multiplexed logic approach, each gate is implemented based on an “executive” unit and a “restorative” unit. The “executive” unit is constructed based on a multiplexed logic unit in which each logic gate is duplicated  $N$  times and each input and output is also duplicated  $N$  times. The inputs randomly pair to feed the  $N$  gates. The “restorative” unit is comprised of two cascaded multiplexed logic units as shown in Figure 1 for a two-input NAND gate, with  $N=4$ . The “restorative” unit is intended to restore some of the incorrect values of the gates to their correct values. It is assumed that the each gate has a probability of failure  $\epsilon$  and that the logic state of the bundle is decided based on the fraction of wires having a specific value above or below a preset threshold. In general, von Neumann’s construction requires a large amount of redundancy and a low error rate for individual gates. It is shown in [20] that for deep logic with a gate failure probability  $\epsilon=0.01$  and  $N=100$ , it is possible to achieve circuit failure probability in the order of  $10^{-6}$ . This required amount of redundancy is excessive and is considered impractical. In order to reduce this large amount of redundancy, the work in [21, 22] combines NAND multiplexing with reconfiguration.

Another defect-tolerant approach is known as the  $N$ -tuple modular redundancy (NMR) in which each gate is duplicated  $N$  times (where  $N$  must be an odd number) followed by an arbitration unit deciding the correct value based on majority. Triple-modular redundancy (TMR) is a special case of NMR. The reliability of such designs is limited by that of the final arbitration unit, making the approach difficult in the context of highly integrated nanosystems [8]. A TMR circuit can be further triplicated. The obtained circuit thus has nine copies of the original module and two layers of majority gates. This process can be repeated if necessary, resulting in a

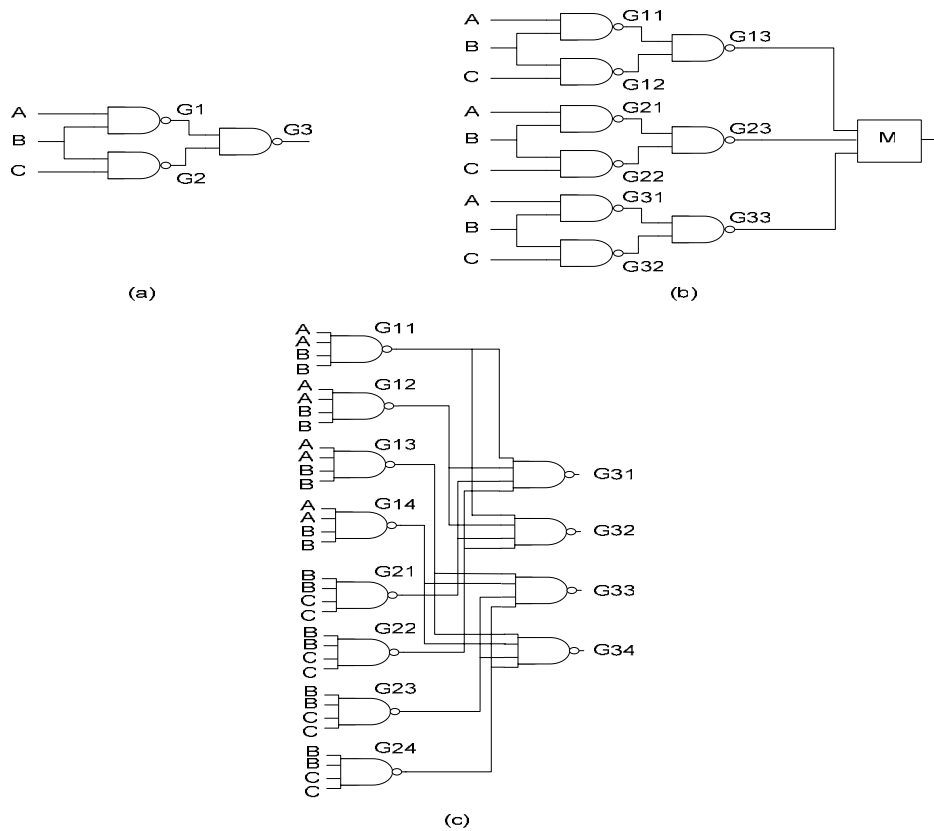


Figure 2 (a) Original circuit, (b) TMR circuit, (c) Quadded logic circuit.

technique called cascaded triple modular redundancy (CTMR) or recursive triple modular redundancy (RTMR). Spagocci and Fountain [12] have shown that using CTMR in a nanochip with large nanoscale devices would require an extremely low device error rate. In [13], it is shown that recursive voting leads to a double exponential decrease in a circuit's failure probability. However, a single error in the last majority gate can cause an incorrect result, hampering the technique's effectiveness. Pierce [10] introduced a fault-tolerant technique called interwoven redundant logic. Quadded logic [11, 14-15] is an ad hoc configuration of the interwoven redundant logic. It requires four times as many circuits. A quadded circuit implementation based on NAND gates replaces each NAND gate with a group of four NAND gates, each of which has twice as many inputs as the one it replaces. While quadded logic guarantees tolerance of most single errors, errors occurring at the last

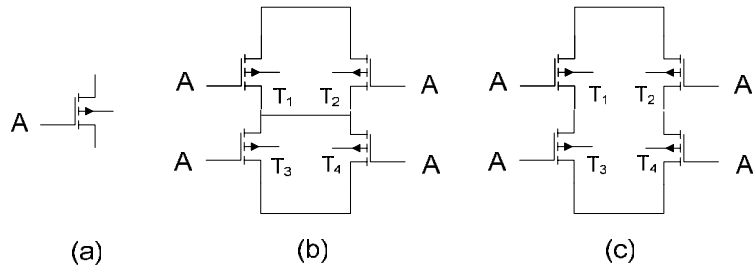


two stages of logic may not be corrected. Figure 2 shows an example of TMR and quadded logic circuits.

Moore et al. [23] have analyzed the use of series-parallel and bridge configurations for the application of redundancy to relay networks. Suran [24] has evaluated the reliability of the quad-relay structure shown in Figure 3(b) and has shown its application using bipolar junction transistors. However, only the reliability of a single structure is evaluated and no extensive circuit reliability analysis is made.

## **2.2 Defect Avoidance Techniques**

Unlike defect-tolerant techniques which are designed to work properly despite the presence of defects, defect avoidance techniques are based on a different principle. They are based on the identification of defective modules and replacing them by other redundant modules through configuration. Mishra and Goldstein [17] have proposed a defect avoidance approach to nanosystem design. This approach is based on a large reconfigurable grid of nanoblocks, each of which can be configured as one of the basic logic building blocks like an AND, an OR, an XOR, a half-adder, and so forth. It maps defects on these nanoblocks, and then synthesizes (offline) a feasible configuration realizing the application for each nanofabric instance. Finally, it configures each instance accordingly. This approach is considered not scalable for large nanosystems as it requires mapping, synthesis, and configuration at such a fine granularity [8]. Furthermore, defect mapping requires unlimited connectivity among nanoblocks. To address the density, scalability, and reliability challenges of emerging nanotechnologies, He et al. [8] proposed a hierarchy of design abstractions, constructed as reconfigurable fabric regions, whereby designers assign small



**Figure 3 (a) Transistor in original gate implementation, (b) First quadded-transistor structure, (c) Second quadded-transistor structure.**

functional flows to each region. The approach demonstrates a tradeoff between yield, delay, and cost in defect-prone nanotechnology-based computing systems.

Various nano-architectures that have been recently proposed are based on a two-dimensional (2D) nano-scale crossbar. The work in [19] has studied the impact of defects on the routability of a crossbar. Results have shown that a defective crossbar can be still utilized at reduced functionality, i.e. as a smaller defect-free crossbar. It is shown that switch stuck-short faults have a significantly higher impact on the manufacturing yield compared to switch stuck-open faults. For this technique to be practical, effective testing and diagnostic techniques are needed to identify defective elements in the crossbar such that they can be bypassed by configuration.

In [25] Tahoori presents an application-independent defect-tolerant design flow where higher level design steps are not needed to be aware of the existence and the location of defects in the chip. Only a final mapping step is required to be defect aware minimizing the number of per-chip design steps, making it appropriate for high volume production. Two algorithms for identifying the maximum defect-free crossbar with the partially defective fabricated crossbar are given.

In [26], Hogg and Snider examined the implementation of binary adders based on defective crossbars. They showed a tradeoff between defect tolerance and circuit area for different implementations. It is shown that the likelihood that defects are tolerable changes abruptly from near one to near zero over a small range of defect rates for a

given crossbar size. Other work has explored defect tolerance in systems composed of multiple crossbars [27, 28].

### **2.3 Defect-Tolerant FPGA Design Techniques**

The regularity of FPGAs makes them suitable candidates for nanotechnology implementation. Reconfigurability in FPGAs has historically been used as means for mitigating the effect of defects. For permanent defects, a recent common practice for the largest two FPGA manufacturers has been to try mapping available designs on working blocks of the FPGA and use it as an "application-specific" FPGA.

The much more widely used fault tolerance application for FPGAs is fault tolerance for transient faults due to single event upsets (SEUs). Until recently, SEUs due to charged particles have been a threat mostly in remote and space computers. With device dimension shrinking to nanometer scales, the threat is now very significant even for terrestrial applications. Asadi et al presented an evaluation for different single-event-upset (SEU) fault tolerance schemes implemented on FPGAs [29].

The bottleneck in triple modular redundancy (TMR) implementations is the voter. The reliability of the system is always limited by that of the voter. Samudrala et al. [30] proposed implementing TMR on FPGAs. They suggest using tri-state buffers (available on Xilinx virtex FPGAs) to build SEU tolerant voters. By doing so, they deal with the bottleneck in the reliability of the TMR. They use a program to evaluate the nodes with a high probability of errors due to SEUs, and selectively implement TMR at the potential gates. The work in [31] investigates the ideal positioning of the voters for a TMR system to achieve maximal robustness with minimal overhead.

TMR is not the only way to deal with SEUs in FPGAs. Some work in the past has compared the efficiency of TMR with that of error detection (using duplication)

followed by recomputing. At low error rates, it is more efficient to use duplication with recomputing. Tiwari et al [32] proposed protecting against SEUs using parity bits in the memory blocks of FPGAs. If an error is detected, the memory is re-written. The technique shows a significant power improvement compared to TMR. Sterpone et al suggest a place and route algorithm to reduce the susceptibility to SEUs in FPGAs [33].

Huang et al in [34, 35] presented a scheme for evaluating the fault tolerance of different FPGAs based on reconfigurability of routing resources in the presence of faulty switches. Routability (a realizable route between input and output endpoints) is used as a measure of fault tolerance. As switches fail, the probability of finding a route between endpoints decreases. The paper uses open and short switches as faults. The work in [36] also investigates routability. The paper proposes a fault-tolerant design for the switch blocks for yield enhancement. The technique is based on wrapping additional multiplexers around the switch blocks to allow different routes for signals. The additional multiplexers lead to higher probability of finding a route between endpoints.

In [37], duplication and concurrent error detection are used to tolerate transient and permanent faults in FPGAs. The paper classifies fault tolerance options in FPGAs as 1) using fault-tolerant blocks, 2) replacing the architecture with a more robust one, or 3) protecting the high level description using redundancy such as TMR, which has been used in the past for such fault tolerance. The authors use time redundancy as well as duplication with comparison. They also apply recomputation with shifted operands and swapped operands. Their technique requires fewer IO pads and consumes less power than TMR. However, it takes more time and requires more flip flops.

The closest previous work to this proposal is in [38]. In this paper, the authors compare coarse and fine-grain redundancy in FPGAs to tolerate defects. For coarse-grain redundancy, they use spare rows and columns, and for fine-grain redundancy they use spare wires. Their findings support using fine-grain redundancy since they offer much higher fault tolerance. They argue that matching the fine-grain fault tolerance using coarse-grain fault tolerance requires double the hardware overhead of fine-grain redundancy, which is about 50%. We believe that the work is quite primitive since it considers only the classical spare rows and columns for coarse-grain redundancy. We also believe that 50% overhead may not be necessary since FPGAs have built-in reconfigurability that can be exploited and are normally substantially underutilized. We intend to consider these factors in our study.

## **2.4 Reliability Analysis**

For proper evaluation of defect tolerant architectures, it is important to rely on reliability analysis techniques that can provide accurate analysis while being efficient.

Recently, several reliability evaluation approaches have been proposed [44-47].

In [44], a probabilistic-based design methodology for designing nanoscale computer architectures based on Markov Random Fields (MRF) is proposed. Arbitrary logic circuits can be expressed by MRF and logic operation is achieved by maximizing the probability of state configurations in the logic network. Markov random network, belief propagation algorithm, and Gibbs energy distribution are selected as the basis for nanoarchitectural approach since its operation does not depend on perfect devices or perfect connections. Successful operation requires that the energy of correct states is lower than the energy of errors.

In [45], the computational scheme based on Markov random field and belief propagation are automated For the evaluation of reliability measures of combinational logic blocks. various reliability results for defect-tolerant architectures, such as triple modular redundancy (TMR), cascaded TMR, and multistage iterations of these are derived.

In [46], a general computational framework based on probabilistic transfer matrices (PTMs) is proposed for accurate reliability evaluation. Algebraic decision diagrams (ADDs) are to improve the efficiency of PTM operations. The proposed approach can be effectively used in exact reliability calculations for analyzing fault-tolerant architectures and in calculating gate error susceptibility.

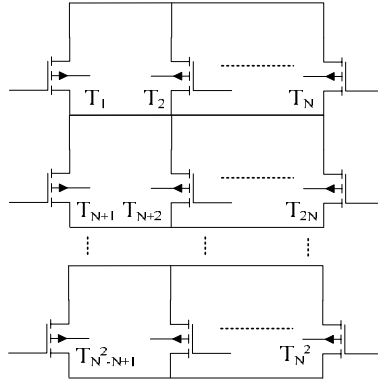
In [47], a method is proposed that enhances the probabilistic gate models (PGMs) for reliability estimation to enable accurate evaluation of reliabilities of circuits. It significantly reduces the PGM method's complexity, making it suitable for practical design-for-reliability applications.

### **3. Methods & Approach**

In this work, we investigate defect tolerance based on adding redundancy at the transistor-level for CMOS circuits. We investigate circuit reliability based on the quadded structure in [24] more thoroughly and generalize it. Our initial results in [41] based on the analysis of defect tolerance of stuck-open and stuck-short defects by the quadded-transistor structure are encouraging and merit further research before the technique is considered viable in practical design. Based on Inductive Fault Analysis defect simulations, it is shown in [40] that over 99% of all the defects in a group of CMOS circuits that caused circuit faults were either bridge or break faults. In this

work, we will extend the analysis to include defect tolerance in the presence of bridging faults. Furthermore, analysis of the  $N^2$ -transistor structure for the case with  $N=3$  and the general case with  $N=k$  will be conducted theoretically and evaluated experimentally.

In the quadded-transistor structure, each transistor  $A$  is replaced by four transistors implementing the logic  $(A+A)(A+A)$  as shown in Figure 3. In order to tolerate single-defective transistors, each transistor,  $A$ , is replaced by a quadded-transistor structure implementing either the logic function  $(A+A)(A+A)$  or the logic function  $(AA)+(AA)$ , as shown in Figure 3. In both of the quadded-transistor structures shown in Figure 3 (b) & (c), any single transistor defect (stuck-open or stuck-short) will not change the logic behavior, and hence the defect is tolerated. Furthermore, double stuck-open defects are tolerated as long as they do not occur in any two parallel transistors ( $T_1\&T_2$  or  $T_3\&T_4$  for the structure in Figure 3(b), and  $T_1\&T_2$ ,  $T_1\&T_4$ ,  $T_3\&T_2$  or  $T_3\&T_4$  for the structure in Figure 3(c)). Double stuck-short defects are tolerated as long as they do not occur in any two series transistors ( $T_1\&T_3$ ,  $T_1\&T_4$ ,  $T_2\&T_3$  or  $T_2\&T_4$  for the structure in Figure 3(b), and  $T_1\&T_3$  or  $T_2\&T_4$  for the structure in Figure 3(c)). In addition, any triple defect that does not include two parallel stuck-open transistors or two series stuck-short transistors is tolerated. Thus, one can easily see that using either of the quadded-transistor structures, the reliability of gate implementation is significantly improved. It should be observed that the effective resistance of the quadded-transistor structures has the same resistance as the original transistor. However, in the presence of a single defect, the worst case effective resistance of the first quadded-transistor structure (Figure 3(b)) is  $1.5R$  while that of the second quadded-transistor structure (Figure 3(c)) is  $2R$ , where  $R$  is the effective resistance of a transistor. This occurs in the case of single stuck-open defects. For



**Figure 4 Defect-tolerant  $N^2$ -transistor structure.**

tolerable multiple defects, the worst case effective resistance of both structures is  $2R$ . For this reason, the first quadded-transistor structure (Figure 3(b)) is adopted in this work.

The quadded-transistor structure, given in Figure 3(b), can be generalized to an  $N^2$ -transistor structure, where  $N=2, 3, \dots, k$ . An  $N^2$ -transistor structure is composed of  $N$  blocks connected in series with each block composed of  $N$  parallel transistors, as shown in Figure 4. An  $N^2$ -transistor structure guarantees defect tolerance of all defects of multiplicity less than or equal to  $(N-1)$  in the structure. Hence, a large number of multiple defects can be tolerated in a circuit implemented based on these structures.

An interesting advantage of the  $N^2$ -transistor structures is that they fit well in existing design and test methodologies. In synthesis, a library of gates implemented based on the quadded-transistor structure will be used in the technology mapping process. The same testing methodology will be used assuming testing is done at the gate-level based on the single stuck-at fault model. So, the same test set derived for the original gate-level structure can be used without any change.

The gate capacitance that the quadded-transistor structure induces on the gate connected to the input  $A$  is four times the original gate capacitance. This has an



impact on both delay and power dissipation. However, as shown in [39], a gate with higher load capacitance has better noise rejection curves and hence is more resistant to soft errors resulting in noise glitches.

In order to tolerate defects in interconnects in the quadded-transistor structure, we propose that four parallel interconnect lines are used to connect the driving gate to the four transistors in a quadded-transistor structure. This guarantees tolerance of any single interconnect defect. This also results in a faster charging of the load capacitance and hence may improve the delay.

In addition to tolerance of permanent defects, design techniques need to cope with transient faults that may occur during circuit operation. Nanometer circuits are also becoming more vulnerable to radiation effects and other sources of soft errors. Single event upsets (SEUs) caused by cosmic ray neutrons or alpha particles severely impact field-level product reliability [43]. However, as shown in [39], only few nodes in the design are considered critical and need to be tolerant to such faults. In this work, we will extend the quadded-transistor structure to handle such soft errors that may occur in the design.

For evaluating circuit failure probability and reliability, we adopt the simulation-based reliability model used in [11]. A complete test set  $T$  that detects all detectable single stuck-at faults in a circuit will be used. To compute the circuit failure probability,  $F_m$ , resulting from injecting  $m$  defective transistors, the following procedure is used:

1. Set the number of iterations to be performed,  $I$ , to 1000 and the number of failed simulations,  $K$ , to 0.
2. Simulate the fault-free circuit by applying the test set  $T$ .
3. Randomly inject  $m$  transistor defects.
4. Simulate the faulty circuit by applying the test set  $T$ .

5. If the outputs of the fault-free and faulty circuits are different, increment  $K$  by 1.
6. Decrement  $I$  by 1 and if  $I$  is not 0 goto step 3.
7. Failure Rate  $F_m = K/1000$ .

Assuming that every transistor has the same defect probability,  $P$ , and that defects are randomly and independently distributed, the probability of having a number of  $m$  defective transistors in a circuit with  $N$  transistors follows the binomial distribution [11] as shown below:

$$P(m) = \binom{N}{m} P^m \times (1-P)^{N-m}$$

Assuming the number of transistor defects,  $m$ , as a random variable and using the circuit failure probability  $F_m$  as a failure distribution in  $m$ , the probability of circuit failure,  $F$ , and circuit reliability,  $R$ , are computed as follows [11]:

$$F = \sum_{m=0}^N F_m \times P(m)$$

$$R = 1 - F = 1 - \sum_{m=0}^N F_m \times P(m)$$

It is well known that the effectiveness of defect-tolerant techniques based on Triple Modular Redundancy is impacted by majority gates. Presence of defects in the majority gates will make the circuit defective. Implementing majority gates using the quadded-transistor structure or the  $N^2$ -transistor structure will significantly enhance their defect tolerance. Combining defect tolerance at both the transistor-level and gate-level is expected to produce promising results. Such an approach will be investigated both theoretically and experimentally in this work.

Another interesting and important aspect of investigation in this work is to compare circuit failure probability for circuits implemented based on the quadded-transistor

structure vs. those implemented using four times the feature sizes based on the same fabrication technology. Both compared circuits will have the same area, speed and power characteristics given the same technology. The question to be answered is which approach will result in more reliable circuits. Inductive fault analysis based on Carafe tool [42] will be used to extract the faults from each of these implementations based on which defect tolerance of both approaches will be compared by simulations. The practicality of the quadded-transistor structure fault-tolerant technique will be investigated through its application to logic designed based on cross-bar switches and the basic combinational logic block (CLB) in field programmable gate arrays (FPGAs). Due to their regularity, crossbar switches are considered the basic building blocks in many recently proposed nano architectures. Comparison between defect avoidance techniques and the proposed transistor-level defect-tolerant technique for crossbar switch designs will be investigated. Furthermore, the study will investigate whether it is more effective to design FPGAs with larger number CLBs such that defective CLBs will be identified and avoided through reconfiguration or to design FPGAs based on a smaller number of defect-tolerant CLBs based on the quadded-transistor structure. It will be assumed that FPGAs in both approaches will occupy the same area.

#### **4. Project Objectives**

The objective of this work is to investigate the design of defect-tolerant digital systems based on redundancy addition at the transistor-level. Defect tolerance based on the quadded-transistor and the  $N^2$ -transistor structures will be analyzed and evaluated both theoretically and experimentally and compared against existing defect tolerance techniques to demonstrate their effectiveness.

To achieve the proposed objectives, the project can be divided into the following tasks:

**Task 1** Extend the probability of failure analysis of the quadded-transistor structure with respect to bridging faults.

**Task 2** Extend the probability of failure analysis of the quadded-transistor structure to the general case of the  $N^2$ -transistor structure with respect to stuck-open, stuck-short and bridging faults.

**Task 3** Experimentally evaluate the impact of the  $N^2$ -transistor structure, for cases  $N=2$  and  $N=3$ , on circuit failure probability in presence of stuck-open, stuck short and bridging faults.

**Task 4** Compare the defect tolerance of circuits implemented based on the  $N^2$ -transistor structure with other defect-tolerance techniques including TMR and quadded logic based defect tolerance techniques.

**Task 5** Implement the Triple Modular Redundancy defect tolerance technique with parametrizable module size to be used for simulations.

**Task 6** Theoretically and experimentally based on simulations evaluate the implementation of Triple Modular Redundancy defect tolerance technique with the majority gate implemented based on the  $N^2$ -transistor structure, with  $N=2$  and  $N=3$ .

**Task 7** Extend the quadded-transistor structure design for tolerance of transient and soft errors and evaluate the design based on simulations.

**Task 8** Based on Inductive Fault Analysis, compare the defect tolerance of circuits implemented based on the quadded-transistor structure and circuits implemented based on transistors of quadruple feature sizes using the same technology.

**Task 9** Investigate applying the quadded-transistor structure for the defect tolerance of logic implemented based on cross-bar switches.

**Task 10** Investigate applying the quadded-transistor structure for the defect tolerance of a generic Combination Logic Block (CLB) in FPGAs. Compare the probability of failure of FPGAs designed based on defect-tolerant CLBs vs. those designed based on regular CLBs with larger count.

**Task 11** Reporting progress reports, final report and publishing papers resulting from proposed work.

## **5. Monitoring & Evaluation**

The time span of this project is twenty four months during which the proposed tasks will be carried out. Table 1 shows a schedule of these tasks indicating the time requirement of each. All team members with the help of two graduate students will participate in all tasks involved in the project. This includes brainstorming discussions, theoretical analysis, analysis and interpretation of experimental results and involvement in implementation aspects.

**Table 1. Work plan timetable.**

| TASK    | Month |     |     |     |      |       |       |       |       |       |       |       |
|---------|-------|-----|-----|-----|------|-------|-------|-------|-------|-------|-------|-------|
|         | 1-2   | 3-4 | 5-6 | 7-8 | 9-10 | 11-12 | 13-14 | 15-16 | 17-18 | 19-20 | 21-22 | 23-24 |
| Task 1  | ↔     |     |     |     |      |       |       |       |       |       |       |       |
| Task 2  | ←     | →   |     |     |      |       |       |       |       |       |       |       |
| Task 3  |       | ←   | →   |     |      |       |       |       |       |       |       |       |
| Task 4  |       |     | ←   | →   |      |       |       |       |       |       |       |       |
| Task 5  |       |     |     | ↔   |      |       |       |       |       |       |       |       |
| Task 6  |       |     |     |     | ←    | →     |       |       |       |       |       |       |
| Task 7  |       |     |     |     |      | ←     | →     |       |       |       |       |       |
| Task 8  |       |     |     |     |      |       | ←     | ——    | →     |       |       |       |
| Task 9  |       |     |     |     |      |       |       | ←     | ——    | →     |       |       |
| Task 10 |       |     |     |     |      |       |       | ←     | ——    | ——    | →     |       |
| Task 11 |       |     | ↔   |     |      | ↔     |       |       | ↔     |       |       | ↔     |

The team will report the progress of the proposed work regularly every six months through progress reports and the final report. Results of this work will be sent for publication as soon as they are available.

**Role of the Consultant:**

Prof. Bashir Al-Hashimi is a well-known scholar with extensive experience in the area of design and test of digital circuits. He will provide consultation for all the planned tasks to be accomplished in the project. He will be involved in some brainstorming discussions and will provide his feedback on the evaluation of all obtained results. Prof. Al-Hshimi will also provide to us the CARAFE tool that we will use for inductive fault analysis which is needed for Task8 in the project. He will also provide consultation on the use of tools and interpretation of the results. In addition, he will also help in accomplishing Tasks 9 and Task 10 and provide to access to necessary FPGA tools that will needed to accomplish these tasks. Task 3-

Task 7 of the project require intensive CPU simulations to asses circuit reliability. Experiments will be conducted both here at KFUPM and University of Southampton to minimize the time needed to obtain the needed evaluations.

The team members have extensive experience in the area of digital system design and test as indicated by their qualifications given below.

**Aiman El-Maleh** is an Assistant Professor in the Computer Engineering Department at King Fahd University of Petroleum & Minerals since September 1998. He holds a B.Sc. in Computer Engineering, with first honors, from King Fahd University of Petroleum & Minerals in 1989, a M.A.SC. in Electrical Engineering from University of Victoria, Canada, in 1991, and a Ph.D in Electrical Engineering, with dean's honor list, from McGill University, Canada, in 1995. He was a member of scientific staff with Mentor Graphics Corp., a leader in design automation, from 1995-1998.

Dr. El-Maleh's research interests are in the areas of synthesis, testing, and verification of digital systems. In addition, he has research interests in VLSI design, design automation, and error correcting codes.

Dr. El-Maleh is the winner of the best paper award for the most outstanding contribution in the field of test for 1995 at the European Design & Test Conference. His paper presented at the 1995 Design Automation Conference was also nominated for best paper award. He holds one US patent.

Dr. El-Maleh was a member of the program committee of the Design Automation and Test in Europe Conference (DATE'98). He is currently serving in the editorial board of the IET Proceedings: Computer and Digital Techniques.

**Ahmad Al-Yamani** is an assistant professor in the computer engineering department at King Fahd University of Petroleum and Minerals. He received a PhD in Electrical Engineering and an MSc in Management Science and Engineering from Stanford. Before that, he received an MSc and a BSc in Computer Engineering from KFUPM. In 2002 he was appointed as the assistant director of Stanford Center for Reliable Computing and in 2004, he was appointed as a consulting assistant professor in the computer systems lab of the electrical engineering department at Stanford University. Ahmad served as an adjunct faculty at Santa Clara University. He also had some industrial experience in VLSI design and test with the advanced development labs of LSI Logic and in computer networks performance analysis with AMD.

**Bashir Al-Hashimi** is Full Professor of Computer Engineering in the School of Electronics and Computer Science, University of Southampton, where he carries out research in embedded computing systems with particular focus on low-power design and low-cost test. He is Deputy Head of School (Academic), and Principal Investigator of EPSRC (UK) platform grant (£1.5M) on System-on-Chip: Design Methods and Tools. Prior to becoming an academic, he worked in industry for six years designing integrated circuits for consumer electronics. Professor Al-Hashimi is the Editor-in-Chief of the IET Proceedings: Computer and Digital Techniques and on the editorial board of Journal of Embedded Systems, and Journal of Low Power Electronics. He is a member of the executive team of the IEE Microelectronics and Embedded Systems Professional Network, the executive committee of the Design, Automation and Test in Europe (DATE) conference, and the



executive committee of the European Workshop on Microelectronics education. He is the general chair of the 11th IEEE European Test Symposium, and the general chair DATE Friday Workshops (2005 and 2006). Professor Al-Hashimi published over 150 papers and authored and co-authored 4 books on circuit simulation, low power design and test. Recently he edited the IEE Press book, System-on-Chip: Next Generation Electronics. Professor Al-Hashimi is a Fellow of the Institution of Electrical Engineers, and Senior Member of the Institution of Electrical and Electronics Engineers.

## **6. Utilization Plan**

The utility value of this project is many-fold, and includes the following aspects:

1. The results of this research can be used by industry as the results of the investigated methodology can have a significant impact on enhancing manufacturing yield and design reliability at the nano-scale.
2. The proposed work will help in training graduate students in the design of reliable systems at the nano-scale and in conducting research.
3. This work could be the seed of further research involving manufacturing of nano-scale devices to demonstrate the applicability of achieved results.
4. There is a potential of patenting some of the ideas resulting from this work.

## **7. Detailed Budget**

The principle investigator, co-investigator and the consultant will be involved during the whole project duration of 24 months. They will receive payments as per the university regulations. The two graduate students will assist in the implementation aspects of the project. Their total compensation will be (13,200/- per Graduate Student/Research Assistant).

|                                      |                           |
|--------------------------------------|---------------------------|
| Dr. Aiman El-Maleh (PI)              | SR 1,200 X 24 = SR 28,800 |
| Dr. Ahmad Al-Yamani (CO-I)           | SR 1,000 X 24 = SR 24,000 |
| Prof. Bashir Al-Hashemi (Consultant) | SR 1,000 X 20 = SR 20,000 |
| Two Graduate Students                | SR 1,200 X 22 = SR 26,400 |
| Secretary                            | SR 2,000                  |
| <hr/>                                |                           |
| Subtotal                             | SR 101,200                |

Facilities available at KFUPM and University of Southampton will be used at no charge to the project. However, the project requires extensive simulation experiments and hence a high performance desktop computer is required with an estimated amount of SR 6000. Stationary and miscellaneous expenses for consumables such as floppies, CDs, paper, printer toner, etc., will amount to SR 2,000, purchase of literature and books, etc., will require SR 2,500.

A secretary will work for the entire duration of the project. SR 2,000 for payments to secretary will be required.

Individual items of the budget are summarized below:

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|                                 |            |
|---------------------------------|------------|
| Man Power                       | SR 101,200 |
| Desktop Computer                | SR 6,000   |
| Books, other literature         | SR 2,500   |
| Stationary and Miscellaneous    | SR 2,000   |
| Conference Attendance (2 Trips) | SR 20,000  |

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The total cost<sup>1</sup> of the project is estimated to be SR 131,700

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<sup>1</sup> SR 131,700=US\$ 35120.

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# Curriculum Vitae

## Aiman H. El-Maleh

### Personal details

Date of Birth: 4th April 1967  
Nationality: Canadian  
Current address: Department of Computer Engineering  
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### Education

|                                |   |
|--------------------------------|---|
| McGill University, Canada      | PhD Degree (Dean's honor list), 1995<br>Thesis title: "Testability Preservation of Combinational and Sequential Logic Synthesis Transformations." |
| University of Victoria, Canada | M.A.Sc., Electrical Engineering, 1991<br>Thesis title: "Image Compression using One-Dimensional Vector Quantization."                             |
| KFUPM, Saudi Arabia            | B.Sc., (First Hon.), Computer Engineering, 1989   |

### Scholarships and Awards

|  |  |
|--|--|
| <b>Distinguished Teaching &amp; Advising Award</b> | College of Computer Sciences & Engineering, 2001/2002.   |
| <b>DATE Best Paper Award</b>                       | Winner of the best paper award for the most outstanding contribution in the field of Test at the Design Automation and Test in Europe (DATE) Conference, 1995. |
| <b>Max Binz Fellowship</b>                         | McGill University, 1993-94   |
| <b>FCAR Scholarship</b>                            | McGill University, 1993-94   |
| <b>NSERC Scholarship</b>                           | McGill University, 1991-93   |
| <b>University of Victoria Fellowship</b>           | University of Victoria, 1990-91  |
| <b>University of Victoria Best TA Award</b>        | University of Victoria, 1990   |

### Employment Summary

**Assistant Professor:** 08/98 to present, King Fahad University of Petroleum and Minerals  
Taught the following courses: Fundamentals of Computer Engineering (COE 200 & COE 202), Computer Organization and Assembly Programming (COE 205), Computer Architecture (COE 308),

Data and Computer Communications (COE 342), VLSI System Design (COE 360), Design and Modeling of Digital Systems (COE 405), Digital System Testing (COE 464 & COE 545), Synthesis of Digital Systems (COE 561), Seminar (COE 390) and COE Cooperative work (COE 351).

**Member of Scientific Staff:** 05/95 to 08/98, Mentor Graphics Corporation, Wilsonville  
Involved in developing advanced Built-In Self Test techniques for ASICs with embedded cores and high performance data path architectures, with feasibility study on the Intel P6 microprocessor. Furthermore, involved on research and development of partial scan selection algorithms for one-million plus gates designs. In addition, developed a fast sequential learning technique for sequential circuits and demonstrated its applicability in improving the performance of sequential ATPG.

## Publications

1. Aiman El-Maleh, Saqib Khurshid, "Efficient Test Compaction for Combinational Circuits Based on Fault Detection Count-Directed Clustering," IET Proceedings Computers & Digital Techniques, 2007 (accepted).
2. Aiman EL-MALEH, MUSTAFA ALI, Ahmad AL-YAMANI, "A Reconfigurable Broadcast Scan Compression Scheme Using Relaxation Based Test Vector Decomposition," IEEE European Test Symposium 2007 (accepted).
3. Aiman EL-MALEH, Bashir AL-HASHIMI, Ahmad AL-YAMANI, "Defect-Tolerant N<sup>2</sup>-Transistor Structure for Reliable Design at the Nanoscale," IEEE European Test Symposium 2007 (accepted).
4. Aiman El-Maleh, Saqib Khurshid, "Efficient Test Compaction for Combinational Circuits Based on Fault Detection Count-Directed Clustering," IEEE Int. Design and Test Workshop, Nov. 19-20, UAE, 2006.
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8. Aiman El-Maleh, Saqib Khursheed, and Sadiq Sait, "Static Compaction Techniques for Sequential Circuits Based on Reverse Order Restoration and Test Relaxation" IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 25, NO. 11, pp. 2556-2564, NOVEMBER 2006.
9. Sadiq M. Sait, Aiman H. El-Maleh, and Raslan H Al-Abaji, "Evolutionary Algorithms for VLSI Multiobjective Netlist Partitioning," ENGINEERING APPLICATIONS OF ARTIFICIAL INTELLIGENCE 19 (3): 257-268 APR 2006.
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12. Aiman El-Maleh and Yahya Osais, "A Class-based Clustering Static Compaction Technique for Combinational Circuits," The 16th International Conference on Microelectronics, pp. 522 – 525, 6-8 Dec. 2004.
13. Aiman El-Maleh and Yahya Osais, "On Test Vector Reordering for Combinational Circuits," The 16th International Conference on Microelectronics, pp. 772 – 775, 6-8 Dec. 2004.
14. Aiman El-Maleh and Khaled Al-Utaibi, "An Efficient Test Relaxation Technique for Synchronous Sequential Circuits," IEEE Transactions on Computer Aided Design of Integrated Circuits, Vol. 23, No. 6, pp. 933-940, June 2004.
15. Aiman El-Maleh and Yahya Osais, "Test Vector Decomposition Based Static Compaction Algorithms for Combinational Circuits", ACM Transactions on Design Automation of Electronic

- Systems, Volume 8, No. 4, pp. 430-459, October 2003.
16. Aiman El-Maleh, "A Hybrid Test Compression Technique for Efficient Testing of Systems-on-a-Chip," 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
  17. Yahya Osais and Aiman El-Maleh, "A Static Test Compaction Technique for Combinational Circuits Based on Independent Fault Clustering," 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
  18. Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "Enhancing Performance of Iterative Heuristics for VLSI Netlist Partitioning", 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
  19. Aiman El-Maleh and Khaled Al-Utaibi, "An Efficient Test Relaxation Technique for Synchronous Sequential Circuits" Proc. of the 21'th IEEE VLSI Test Symposium (VTS), pp. 179-185, 2003.
  20. Aiman El-Maleh and Khaled Al-Utaibi, " ON EFFICIENT EXTRACTION OF PARTIALLY SPECIFIED TEST SETS FOR SYNCHRONOUS SEQUENTIAL CIRCUITS " Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. V-545 - V-548, 2003.
  21. Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "SIMULATED EVOLUTION ALGORITHM FOR MULTIOBJECTIVE VLSI NETLIST BI-PARTITIONING" Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. V-457 - V-460, 2003.
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35. Sadiq Sait, Habib Yousef, Junaid Khan, and Aiman El-Maleh, "Fuzzy Simulated Evolution for Low power and High Performance Optimization of VLSI Placement", International Joint INNS-IEEE Conference on Neural Networks (IJCNN), pp. 738-743, 2001.
  36. Sadiq Sait, Habib Yousef, Junaid Khan, and Aiman El-Maleh, "Fuzzified Iterative Algorithms for Performance Driven Low Power VLSI Placement", International Conference on Computer Design (ICCD), pp. 484-487, 2001.
  37. Aiman El-Maleh, Mark Kassab, and Janusz Rajski, "A Fast Sequential Learning Technique for Real Sequential Circuits with Application to Enhancing ATPG Performance," in Proc. of 32nd Design Automation Conference, pp. 625-631, June 1998.
  38. Aiman El-Maleh, Thomas Marchok, Janusz Rajski, and Wojciech Maly, "Behavior and Testability Preservation Under the Retiming Transformation," IEEE Transactions on Computer-Aided Design, Vol. 16, pp. 528-543, May 1997.
  39. Wu-Tung Cheng, Aiman El-Maleh, Rob Thompson, Don Ross, and Janusz Rajski, "The Pitfalls of Necessary Assignments", Fourth International Test Synthesis Workshop, May 1997, Santa Barbara, CA.
  40. Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, "A Complexity Analysis of Sequential ATPG," IEEE Transactions on Computer-Aided Design., Vol. 15, pp. 1409-1423, Nov. 1996.
  41. Janusz Rajski, Aiman El-Maleh, and Jerzy Tyszer, "Arithmetic BIST Tackles Embedded Cores," Electronic Engineering Times, Oct. 21, 1996.
  42. Aiman El-Maleh and Janusz Rajski, "Delay Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations," IEEE Transactions on Computer-Aided Design, Vol. 14, pp. 582-590, May 1995. (A special section on 12th IEEE VLSI Test Symposium.)
  43. Thomas Marchok, Aiman El-Maleh, Janusz Rajski, and Wojciech Maly, "Testability Implications of Performance Driven Logic Synthesis," in IEEE Design and Test of Computers, pp. 32-39, summer 1995. (A special issue on First International Test Synthesis Workshop.)
  44. Aiman El-Maleh, Thomas Marchok, Janusz Rajski, and Wojciech Maly, "On Test Set Preservation of Retimed Circuits," in Proc. of the 32nd Design Automation Conference, pp. 176-182, June 1995. (Best paper award nomination.)
  45. Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, "Complexity of Sequential ATPG," in Proc. of the European Design and Test Conference, pp. 252-261, March 1995 (Winner of the best paper award for the most outstanding contribution in the field of test in 1995).
  46. Aiman El-Maleh and Janusz Rajski, "Algebraic Resubstitution with Complement and Testability Preservation," Presented at the First International Test Synthesis Workshop, May 1994, Santa Barbara, CA.
  47. Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, "Test Set Preservation under Retiming Transformation," Presented at the First International Test Synthesis Workshop, May 1994, Santa Barbara, CA.
  48. Aiman El-Maleh and Janusz Rajski, "Delay-Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations," in Proc. of IEEE VLSI Test Symposium, April 1994, pp. 15-21.
  49. Janusz Rajski, Jagadeesh Vasudevamurthy, and Aiman El-Maleh, "Recent Advances in Logic Synthesis with Testability," in Proc. of IEEE VLSI Test Symposium, April 1992, pp. 254-256.
  50. Aiman H. El-Maleh, Fayez El-Guibaly, and V.K. Bhargava, "Improving the Performance of One-Dimensional Vector Quantization Using Product Structures," in Proc. of the 1991 First Cyprus International Conference on Computer Applications to Engineering Systems, Nicosia, Cyprus, July 1991, pp. 40-45.
  51. Aiman H. El-Maleh, Fayez El-Guibaly, and V.K. Bhargava, "A Comparison of One- And Two-Dimensional Vector Quantization of Images," in Proc. of the 1991 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, Canada, Vol. 2, May 1991, pp. 490-493.
  52. Aiman H. El-Maleh and Sadiq M. Sait, "A State Machine Synthesizer With Weinberger Arrays," in Proc. of the 1991 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, Canada, Vol. 2, May 1991, 753-756.

53. Sadiq M. Sait and Aiman H. El-Maleh, "State Machine Synthesis with Weinberger Arrays," *Int. Journal of Electronics*, Vol. 71, No. 1, pp. 1-12, July 1991.

## Patents

*Aiman H. El-Maleh, Wojciech Maly, Thomas E. Marchok, Janusz Rajski, "Test Pattern Generation for an Electronic Circuit Using a Transformed Circuit Description," US Patent 5,528,604.*

## Thesis Supervision

1. Syed Zafar Shazli, Experimenting with Iterative Heuristics for State Justification in Sequential ATPG, M.Sc., Nov. 1998-Apr. 2001 (Supervisor).
2. Esam Khan, A Two-Dimensional Geometric-Primitives-Based Compression Scheme for Testing Systems-on-a-Chip, M.Sc., Nov. 1999-May 2001 (Supervisor).
3. Ali Al-Suwaiyan, An Efficient Test Vector Relaxation Technique for Combinational Circuits, M.Sc., June 2000-May 2002 (Supervisor).
4. Khaled Al-Utaibi, An Efficient Test Relaxation Technique for Sequential Circuits, M.Sc., Nov. 2000-May 2002 (Supervisor).
5. Raslan Al-Abaji, Evolutionary Techniques for Multi-Objective VLSI Netlist Partitioning, M.Sc., July 2001-May 2002 (Co-supervisor).
6. Yahya I. Osais, Efficient Static Compaction Algorithms for Combinational Circuits Based on Test Relaxation, M.Sc., Sep. 2001-Oct. 2003 (Supervisor).
7. Syed Saqib Khursheed, Test Set Compaction for Sequential Circuits based on Test Relaxation, M.Sc., Oct. 2003-Dec. 2004 (Supervisor).
8. Faisal Nawaz Khan, Finite State Machine Encoding/State Assignment for Low Power, Reduced Area and Increased Testability using Iterative Algorithms, M.Sc., Oct. 2003-June 2005 (Supervisor).
9. Mustafa Imran Ali, An Efficient Relaxation-based Test width compression technique for multiple scan chain testing, M.Sc., June 2005-Sep. 2006 (Supervisor).

# CURRICULUM VITAE

AHMAD A. AL-YAMANI

## EXPERIENCE

---

**July 1997 – present**                      **KFUPM, Dhahran, Saudi Arabia**

*Assistant Professor, Computer Engineering (Oct 2005 – present)*

*Lecturer, Computer Engineering (June 1999 – Oct 2005)*

*Graduate Assistant, Computer Engineering (July 1997 – June 1999)*

1. Teaching introduction to computer engineering, computer networks, fundamentals of computer communications, personal computers, digital system design, and digital systems testing.
2. Conducting funded research and mentoring graduate students in digital systems design and test, design for testability, built-in self test, nanotechnology and reliable computing.
3. Participating in several administrative committees at all levels within KFUPM.

**June 2004 – Aug 2006**    **Stanford University, Stanford, CA, USA**

*Consulting Assistant Professor, Electrical Engineering*

- Taught graduate/undergraduate logic design at Stanford University.
- Mentored the research of two PhD students.
- Co-raised/extended over \$2 million grants with Professor McCluskey.

**Dec 2001 – Aug 2006**    **Stanford University, Stanford, CA, USA**

*Assistant Director, Stanford Center for Reliable Computing*

- Led the design team of the ELF13 test chip (130 nanometer, 4M gates).
- Led the testing and analysis of the ELF35 test chip (0.35  $\mu$ , 0.5M gates).

**April 2004 – Aug 2006**    **Santa Clara University, Santa Clara, CA, USA**

*Adjunct Faculty, Electrical Engineering*

- Taught a graduate class on logic analysis and synthesis.

**Jun 2004 – Jul 2005**                      **LSI Logic Corporation, Milpitas, CA, USA**

*Staff Engineer, Advanced Development Labs*

4. Led a major test cost saving operation with \$1.6M of annual projected savings based on new patent-pending technologies.
  5. Supervised two research projects at Stanford University. One funded by LSI Logic directly and the other through Semiconductor Research Corporation.
- Co-disclosed 6 patents (4 of them already filed, 2 as 1<sup>st</sup> inventor).

**Summer 2006**                                      **University of Bristol, Bristol, UK**

*Research Associate, Computer Science*

- Worked on several research projects in nanotechnology and reliable computing, and delivered tutorials on digital systems testing and synthesis.

**Summer 2000**                                      **AMD Inc., Sunnyvale, CA, USA**

*Computer Networks Performance Consultant, Advanced Design Labs*

- Worked on simulating and evaluating aspects of Home Phone-Line Networks.

**Summer 1996 MIC-Proctor and Gamble, Dammam, Saudi Arabia**

*Systems Analyst, Management Systems*

- Developed three database systems in Access: Manufacturing Expense Report Tracking System, Medical Claims System and Employees Attendance System

**EDUCATION**

---

**1999–2004**

**Stanford University, Stanford, CA, USA**

6. Ph.D., Electrical Engineering - Concentration on VLSI design and test, design for testability, built-in self-test, and fault-tolerant computing.
- M.Sc., Management Science and Engineering - Concentration on network systems. Courses on decision analysis, strategy, organizational behavior, optimization, and accounting.

**1992–1999**

**King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia**

7. M.Sc., Computer Engineering - Concentration on VLSI physical design automation and parallel iterative heuristics.
- B.Sc., Computer Engineering.

**HONORS AND AWARDS**

---

8. Selected to appear in *Who's Who of Emerging Leaders* 2007 (featuring 25,000 men and women under the age of 40 who represent the best of a new generation of leaders worldwide).
9. Winner of the British Council summer research award for 2006.
10. Patent champion of LSI Logic (2005) for disclosing 6 patents in less than a year.
11. First recipient of Gerald Gordon international award from the IEEE test technology technical council, 2003; for role in organizing the Pacific Northwest test workshop.
12. Two awards for contribution to Pacific Northwest test workshop 2002, and 2003
13. Over 15 research publication awards from the Saudi Arabian Cultural Mission in Washington, 2000 – 2005.
14. "Best graduate assistant award" in computer engineering at KFUPM 1997.
15. Highest honor list at KFUPM, 1992 – 1997.
16. Several certificates of appreciation from KFUPM for distinct efforts and active contribution in students' activities, 1992 – 1997.

**RESEARCH AND DEVELOPMENT**

---

Involved in research in VLSI design and test, design-for-testability, built-in self-test, nanotechnology electronics reliability, computer-aided design automation, iterative heuristics and their parallelization for VLSI design, and reliable computing. Publications below reflect the extent of involvement in each area.

**MS THESES COMMITTEES:**

1. Mustafa Imran, "*Test Data Volume Reduction of Scan-Based Deterministic Test based on Scan Chains Compatibility using Partitioning & Relaxation*," M.Sc. Thesis, King Fahd University of Petroleum and Minerals, 2006 (Member).
2. Ali Zaidi, "*An efficient reconfigurable architecture for secret and public key cryptography*," M.Sc. Thesis, King Fahd University of Petroleum and Minerals, 2007 (Member).

**FUNDED PROJECTS:**

3. "*Scan Test Cost and Power Reduction through Systematic Scan Reconfiguration*," KFUPM funded project, 2006-2007 (Primary Investigator).
4. "*Test Data Volume Reduction of Scan-Based Deterministic Test based on Scan Chains Compatibility using Partitioning & Relaxation*," Sabic funded project, 2006-2007 (Co-Investigator).

5. "Energy-Delay Efficient Test," BAE, British Council, and KFUPM funded project, 2006 (Primary Investigator).

#### **PUBLICATIONS:**

##### THESES:

1. Ahmad Al-Yamani, "A Parallel Tabu Search Algorithm for VLSI Standard Cell Placement," M.Sc. Thesis, King Fahd University of Petroleum and Minerals, June 1999.
2. Ahmad Al-Yamani, "Deterministic Built-In Self Test for Digital Circuits," Ph.D. Thesis, Stanford University, April 2004.

##### JOURNALS:

3. Al-Yamani, A.A., S. Sait and H. Youssef, "Parallelizing Tabu Search on a Cluster of Heterogeneous Workstations," *Journal of Heuristics on Parallel Metaheuristics*, 8(3), pp. 277-304, May 2002.
4. Al-Yamani, A.A., S. Mitra, and E.J. McCluskey, "Optimized Reseeding by Seed Ordering and Encoding," *IEEE Transactions on Computer-Aided Design (TCAD'05)*, 24(2), pp. 264-271, February 2005.
5. Al-Yamani, A.A, and E.J. McCluskey, "Test Chip Experimental Results on High Level Structural Test," *ACM Transactions on Design Automation of Electronic Systems (TODAES'05)*, October 2005. (INVITED)
6. Al-Yamani, A., N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, "Scan Test Cost and Power Reduction through Systematic Scan Reconfiguration," **Accepted for IEEE Transactions on Computer-Aided Design**

##### CONFERENCES AND SYMPOSIA:

7. S. Sait, Youssef, Barada, and A. Al-Yamani, "A Parallel Tabu Search Algorithm for VLSI Standard Cell Placement," *IEEE International Symposium on Circuits and Systems (ISCAS'00)*, Geneva, Switzerland, May 2000.
8. Al-Yamani, A.A., N. Oh, and E.J. McCluskey, "Algorithm-Based Fault Tolerance: A Performance Perspective Based on Error Rate," Fast Abstract, *IEEE International Symposium on Dependable Systems and Networks (DSN'01)*, Gotenberg, Sweden, July 1-4, 2001.
9. Al-Yamani, A.A., N. Oh, and E.J. McCluskey, "Performance Evaluation of Checksum-Based ABFT," *16th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'01)*, San Francisco, CA, Oct. 24-26, 2001.
10. Al-Yamani, A.A., S. Mitra, and E.J. McCluskey, "Techniques for Testing Digital Circuits with Constraints," *17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'02)*, Vancouver, Canada, Nov. 6-8, 02.
11. Al-Yamani, A.A., S. Sait and H. Barada, "HPTS: Heterogeneous Parallel Tabu Search for VLSI Placement," *IEEE Congress on Evolutionary Computing (CEC02)*, Honolulu, Hawaii, May 12-17, 2002.
12. Al-Yamani, A.A., S. Sait, H. Youssef, and H. Barada, "Parallel Tabu Search in a Heterogeneous Environment," *IEEE International Parallel and Distributed Processing Symposium (IPDPS'03)*, Nice, France, Apr. 22-26, 2003.
13. Al-Yamani, A.A., and E.J. McCluskey, "Built-In Reseeding for Serial BIST," *21st IEEE VLSI Test Symposium (VTS'03)*, Napa Valley, CA, Apr. 27-May 1, 2003.
14. Al-Yamani, A.A., S. Mitra, and E.J. McCluskey, "BIST Reseeding with Very Few Seeds," *21st IEEE VLSI Test Symposium (VTS'03)*, Napa Valley, CA, Apr. 27-May 1, 2003.
15. Al-Yamani, A.A., and E.J. McCluskey, "Seed Encoding for LFSRs and Cellular Automata," *40th ACM/IEEE Design Automation Conference (DAC'03)*, Anaheim, CA, June 2-6, 2003.
16. McCluskey, E.J., A. A. Al-Yamani, C.-M. Li, C.W. Tseng, E. Volkerink, F. Ferhani, E. Li, and S. Mitra, "ELF-Murphy Data on Defects and Test Sets," *22nd IEEE VLSI Test Symposium (VTS'04)*, Napa Valley, CA, Apr. 25-28, 2004.



17. Salama, K.N., and A.A. Al-Yamani, " Analysis of Self-Correcting Active Pixel Sensors," *SPIE's 17th Annual Symposium on Electronic Imaging Science and Technology*, San Jose, CA, January 2005.
18. Al-Yamani, A.A., and E.J. McCluskey, "BIST-Guided ATPG," *6<sup>th</sup> IEEE International Symposium on Quality Electronics Design (ISQED'05)*, San Jose, CA, March 21-23, 2005.
19. Al-Yamani, A.A., Erik Chmelar and Mikhail Grinchuk, "Segmented Addressable Scan Architecture," *23<sup>rd</sup> IEEE VLSI Test Symposium (VTS'05)*, Palm Springs, CA, May 1-5, 2005.
20. Park, I., A. Al-Yamani, and E.J. McCluskey, "Effective TARO Pattern Generation," *23<sup>rd</sup> IEEE VLSI Test Symposium (VTS'05)*, Palm Springs, CA, May 1-5, 2005.
21. Al-Yamani, A., N. Devta-Prasanna, and A. Gunda, "Should Illinois-Scan Architectures be Centralized or Distributed," *IEEE International Symposium on Defect and Fault Tolerance (DFT'05)*, Monterey, CA, Oct 3-5, 05.
22. Al-Yamani, A "DFT for Controlled-Impedance IO Buffers," *43rd ACM/IEEE Design Automation Conference (DAC'06)*, San Francisco, CA, July 24-26, 2006
23. Al-Yamani, A., N. Devta-Prasanna, and A. Gunda, "Systematic Scan Reconfiguration," *12<sup>th</sup> IEEE Asia and South Pacific Design Automation Conference (ASPDAC'07)*, Yokohama, Japan, Jan 23-26, 2007.
24. Ramsundar, S., A Al-Yamani and D. Pradhan, "Defect Tolerance in Nanotechnology Switches Using a Greedy Reconfiguration Algorithm," *IEEE International Symposium on Quality Electronics Design (ISQED'07)*, San Jose, CA, March 26-28, 2007.
25. El-Maleh, A., B. Al-Hashimi, and A. Al-Yamani, "N2-Transistor Structure for Defect-Tolerance at the Nanoscale," *IEEE European Test Symposium (ETS'07)*, Freiburg, Germany, May 20-24, 2007

#### WORKSHOPS:

26. Al-Yamani, A.A., and E.J. McCluskey, "Low-Overhead Built-In BIST Reseeding," *3rd IEEE International Workshop on Test Resource Partitioning (TRP'02)*, Baltimore, MD, Oct. 10-11, 2002.
27. Al-Yamani, A.A., and E.J. McCluskey, "Test Quality for High Level Structural Test," *IEEE High Level Design Validation and Test (HLDVT'04)*, Sonoma, CA, November 2004.
28. Al-Yamani, A.A., "Test Time Reduction through Power Control," *IEEE International Design and Test (IDT'06)*, Dubai, UAE, November 2006.
29. Argyrides, C, J. Mathew, A. Al-Yamani, and D. Pradhan, " Performance Analysis of an Error Tolerant Low Power Memory Architecture," *IEEE International Design and Test (IDT'06)*, Dubai, UAE, November 2006.
30. Argyrides, C, D Pradhan, and A Al-Yamani, "Non-square Meshes for Improved Yield in Nanotechnology Circuits," *IEEE Latin-American Test Workshop (LATW'07)*, Cuzco, Peru, Mar 07.
31. El-Maleh, A., B. Al-Hashimi, and A. Al-Yamani, "Defect-Tolerant N2-Transistor Structure for Reliable Design at the Nanoscale," *IEEE Workshop on Robust Computing with Nano-scale Devices: Progresses and Challenges*, Nice, France, Apr 16-20, 2007

#### TECHNICAL REPORTS:

32. Al-Yamani, A.A., S. Mitra, and E.J. McCluskey, "Avoiding Illegal States in Pseudorandom Testing of Digital Circuits," *Stanford CRC TR 02-02*.
33. Al-Yamani, A.A., and E.J. McCluskey, "Built-In Reseeding for Built-In Self Test," *Stanford CRC TR 02-03*.

#### PATENTS:

34. Grinchuk, M., A. A. Al-Yamani, and E. Chmelar, "System And Method For Implementing Postponed Quasi-Masking Test Output Compression In Integrated Circuit," **Filed with USPTO**, Dec 16, 2004, Application number 20060156128.
35. Al-Yamani, A. A., M. Grinchuk, and E. Chmelar, "Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits,"

**Filed with USPTO**, March 31, 2005, Application number 20060236176.

36. Al-Yamani, A. A., N. Devta-Prasanna, and A. Gunda, "Systematic Scan Reconfiguration," **Filed with USPTO**, April 26, 2005, Application number 20060242515.
37. Grinchuk, M., A. A. Al-Yamani, and E. Chmelar, "Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits," **Filed with USPTO**, May 18, 2005, Application number 20060282728.

#### **TECHNICAL PRESENTATIONS:**

Presented all 1<sup>st</sup> author papers in their corresponding conferences and workshops and was invited to give several technical presentations to high-tech companies and workshops in the silicon valley, and to some universities in the US and the UK.

#### **REFEREEING:**

Ahmad is a referee for the following journals and conferences:

- IEEE Transactions on Computer Aided Design
- IEEE Transactions on Computers
- ACM Transactions on Design Automation of Electronic Systems
- Elsevier Journal of Systems and Software
- Springer Journal of Electronic Testing Theory and Applications
- Springer International Journal of Parallel Programming
- The Arabian Journal for Science and Engineering
- IEEE International Test Conference
- IEEE VLSI Test Symposium
- IEEE Design Automation Conference
- IEEE International Design and Test Conference

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#### **ADMINISTRATIVE AND ORGANIZATIONAL WORK**

#### **COMMITTEES:**

- Aafaq – Strategic plan for higher education in Saudi Arabia (Country), IT Champion
- Information and communication technology committee (University)
- Nanotechnology group formation committee (University)
- Center of Excellence in Nanotechnology committee (University)
- E-government committee (University)
- IT client companies committee (University)
- Students fund council (University)
- VIP committee (University)
- Career day committee (University)
- British Council program evaluation committee (University)
- Outreach committee (College)
- Industrial relations committee (Department)
- Industrial advisory board (Department)
- Publicity and information committee (Department)

#### **JOURNALS, CONFERENCES AND WORKSHOPS:**

- Member of editorial board for the Open Electrical and Electronics Engineering Journal.
- Member of the program committee for the IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS).
- Member of the scientific committee and session chair for the 18th IEEE International Conference on Microelectronics (ICM'06).
- Member of the technical committee for the 2nd Symposium on E-Services in the Eastern Province (ESS'07).
- Member of the program committee for the 1st IEEE International Design and Test workshop (IDT'06).
- Member of the organizing committee for the 12th and the 13th IEEE Pacific Northwest Test Workshop (BAST'03 and BAST'04).
- Member of the organizing committee for the special workshop in honor of Professor McCluskey in conjunction with the International Conference on Computer Design'04.

- Member of the program committee for 14th IEEE Pacific Northwest Test Workshop (BAST'05).

**PROFESSIONAL ORGANIZATIONS:**

- Member of IEEE, IEEE Computer Society, and Circuits and Systems Society.
- Member of Saudi Engineers Council.

**SOFTWARE SKILLS**

---

- C, Perl, Pascal and Fortran Programming.
- Verilog (Hardware Description Language).
- MATLAB
- Synopsys: Design Compiler, Behavioral Compiler, and Test Generator.
- SIS (UC Berkeley Synthesis Tool).
- Magic (VLSI Layout tool).
- DFT and ATPG tools of Synopsys, Mentor Graphics, SynTest, and Virginia Tech.

**LANGUAGES AND PERSONAL INFORMATION**

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- Fluent Arabic and English and beginning French.
- Hobbies include squash, volleyball and swimming.
- Proud to have co-authored papers with 20 different people from 14 different countries and 6 different continents.

**REFERENCES**

---

- Available upon request.

# *Curriculum Vitae*

## **Bashir M. Al-Hashimi, FIEE, SMIEE**

### **Personal details**

Date of Birth: 5th January 1962  
Nationality: British  
Current address: School of Electronics and Computer Science  
University of Southampton, Southampton SO17 1BJ, UK  
WWW: <http://www.ecs.soton.ac.uk/~bmah>  
E-mail: [bmah@ecs.soton.ac.uk](mailto:bmah@ecs.soton.ac.uk)  
Phone: +44 (0) 2380593249  
Fax: +44 (0) 23 80592901  
Office: Building 86, Room 1013

### **Education**

University of York, UK PhD Degree, 1989  
Thesis title: CMOS Design of High Frequency Analogue Filters  
University of Cardiff, UK MSc Electronic Engineering (Distinction), 1985  
University of Bath, UK BSc, 1st-class (Hons), Electrical and Electronic Engineering, 1984

### **Employment Summary**

October 1999 - Present  
Professor of Computer Engineering, Director of Pervasive Systems Research Center, Deputy Head of School (Academic), School of Electronics and Computer Science, Southampton University, UK  
January 1994 - September 1999  
Principal Lecturer, Postgraduate Awards Manager, Head of VLSI Signal Processing Group, School of Engineering, Staffordshire University  
June 1991 - December 1993  
Team leader (Electronics Systems), Johnson Matthey, Stoke-on-Trent  
June 1989 - May 1991  
Philips Semiconductors, IC Design Engineer, Southampton

### **Research**

My expertise lies in the development of algorithms and architectures that underpin the design automation of complex electronics with particular emphasis on low-power efficient embedded computing systems needed in mobile telecommunications, consumer electronics, and other areas of pervasive computing. At present I lead a research team of 6 post doctoral researchers, 6 PhD students, 2 visiting professors and 2 visiting researchers.

#### **Summary of significant personal achievements in research and scholarship**

- Authored and co-authored over 180 journal and refereed conference papers
- Total research and development income in the excess of £3.5M, including a prestigious EPSRC/UK platform grant: SoC Design Methods and Tools, Jul.04-Jul.07, and Electronics Design.
- I was invited by the IEE Press to edit the book “System on Chip: Next Generation Electronics”. The book has 25 chapters from leading research groups world-wide. The book is 950 pages and presents the most comprehensive and up to date survey of the latest development in the area.
- Co-authored two research books: “System Level Design Techniques for Energy Efficient Embedded Systems”, 2004, and “Power Constrained Testing of VLSI Circuits”, 2003

- Best paper award with N. Nicolici at the International Test Conference, 2000. Two best paper nominations at DATE 03 and 04 and a best paper nomination at ETS04, see publication list
- 16 Successful PhD theses supervision
- Editor-in-Chief, IEE Proceedings: Computers and Digital Techniques, Sep.02
- Member of Editorial Board of:
  - Journal of Embedded Computing, (Cambridge International Science Pub.), Jan.03 -
  - Journal of Low Power Electronics, (American Science Pub.), Sept.05 -
  - Journal of Electronic Testing: Theory and Application, (Springer), Jan.06
  - Transactions on VLSI Systems, IEEE, Oct.02 - Sep.05
- Executive and Steering committee member of numerous international conferences, including DATE, ETS and CODES/ISSS, and the IEE PN “Embedded Microelectronics Systems”
- Member of EPSRC Peer Review College

## Teaching

I have strong interest and track record in developing educational programmes that underpin my research activities, of interest to students and of relevance to industry. My teaching interests: electronics design (digital systems, VHDL, FPGA), embedded systems, CAD tools and simulation.

### Summary of significant personal achievements in Education and administration

- Deputy Head of School (Academic), Oct.04
- Development of MSc course “System-on-Chip”, Oct.05, current student number 50
- Text book on SPICE simulation, Jan.95, with over 6000 copies sold world-wide. The book translated to Italian (97) and Japanese (97)
- IEE Accreditation (Electronics and Computer Eng., Course Leader), rating “Exemplar”, Apr.03
- Developed and run industrial short courses, including securing EPSRC funding for development
- Steering committee member of the European Microelectronics Education Workshop

## Referees

Professor Wendy Hall CBE FREng  
 Head of Electronics and Computer Science School  
 University of Southampton, Southampton SO17 1BJ, UK  
 E-mail: [wh@ecs.soton.ac.uk](mailto:wh@ecs.soton.ac.uk)  
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Professor J.K. Fidler  
 Vice-Chancellor, University of Northumbria at Newcastle  
 Newcastle NE1 8ST, UK  
[kel.fidler@unn.ac.uk](mailto:kel.fidler@unn.ac.uk)

Professor Krishnendu Chakrabarty  
 Electrical and Computer Engineering  
 Duke University, Durham, NC 27708, US  
[krish@ee.duke.edu](mailto:krish@ee.duke.edu)

Professor Petru Eles  
 Embedded Systems Laboratory (ESLAB)  
 Department of Computer and Information Science  
 Linköping University, SWEDEN  
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# Publications

## Books and Edited Work

1. Bashir M. Al-Hashimi (Editor), System-on-Chip: Next Generation Electronics, IEE Press, Circuits and Systems Series, 944pp, Jan.06, ISBN 0863415520 (Invited by the IEE Press)
2. Marcus Schmitz, Bashir M. Al-Hashimi, Petru Eles, System-Level Design Techniques for Energy-Efficient Embedded Systems”, Kluwer Academic Publishers, 200pp, Jan.04, ISBN 1402077505
3. Bashir M. Al-Hashimi, Nicola Nicolici, Power Constrained Testing of VLSI Circuits, Kluwer Academic Publishers, Frontiers in Electronic Testing Series, 180pp, Jan.03, ISBN 140207235
4. Bashir M. Al-Hashimi, The Art of Spice Simulation, Analog and Digital, CRC Press, 248pp, ISBN 08493-78958, Jan.95. Italian and Japanese translation in 1997

## Special Issues

1. Low Power Systems-on-Chip, with Prof. E. Macii (Politecnico di Torino), and Prof. K. Roy (Purdue University), IEE Proceedings- Computers and Digital Techniques- A Special Issue, ISSN 1350-2387, Vol.149, No.4, Jul.02
2. Embedded Systems Design in the UK, Kluwer International Journal: Design Automation for Embedded Systems, ISSN 0929-5585, Vol.6, No.4, Jul.02. (Invited by Prof. W. Wolf, Princeton Uni.)
3. Embedded Microelectronics Systems: Status and Trends, IEE Proceedings- Computers and Digital Techniques, ISSN 1350-2387, 152(2-3), pp.113-390, March/May 2005

## Books Contributions

1. Chapter on “Computer Based Circuit Simulation”, CRC Press/ IEEE Press book “The Electronics Handbook”, Editor J.C. Whitaker, ISBN 0849383455, 1996
2. Chapter on “Electronics System Simulation”, CRC Press/ IEEE Press book “The Electronics Systems Maintenance Handbook”, 2001
3. Chapter on “Energy-Efficient Embedded Computing Systems”, with P. Eles, Springer book “Embedded systems for SoCs), Henkel (Editor), 2006

## Journals

(Copies are available, <https://ecs.soton.ac.uk/~bmah>)

1. Cai, Y., Schmitz, M., Al-Hashimi, B.M., S. Reddy, “Workload-Ahead-Driven online Energy Minimization Techniques for Battery-Powered Embedded Systems with Time Constrained”, ACM Transactions on Design Automation of Electronics Systems, 12(1), pp.1-25, Jan. 2007.
2. Ejlali, A., Al-Hashimi, B. M., Schmitz, M., Rosinger, P. and Miremadi, S. G. ”Combined Time and Information Redundancy for SEU-Tolerance in Energy-Efficient Real-Time Systems”, IEEE Transactions on VLSI Systems, 14(4), pp.323-335, Apr.2006
3. Rosinger, P., Al-Hashimi, B. M. and Chakrabarty, K. “Thermal-Safe Test Scheduling for Core-Based System-on-Chip Integrated Circuits”, IEEE Transactions on CAD, 25(11), pp.2502-2512, Nov.2006
4. Varea, M., Al-Hashimi, B. M., Cortés, L. A., Eles, P. and Peng, Z. “Dual Flow Nets: Modelling the Control/Data-Flow Relation in Embedded Systems”, ACM Transactions on Embedded Computing Systems (TECS), 5(1), pp.1-29, Apr.06
5. Collins, M., Al-Hashimi, B.M., Wilson, P., “On-Chip Timing Measurements with Femtosecond Resolution” IEE Electronics Letters, 42(9), pp. 528-530, April 06
6. Wurtenberger, A., Rosinger, P., Al-Hashimi, B.M., Chakrabarty, K, “Cost Model Driven Test Resource Partitioning for SoCs”, IEE Electronics Letters, Vol.42, No.16 pp. 915-916, Aug.06
7. Dilillo, L., Rosinger, P., Al-Hashimi, B. M. Girard, P, "Reducing Power Dissipation in SRAM during Test", Journal of Low Power Electronics, 2(2), pp.271-280, Aug. 2006
8. Gonciari, P. T., Al-Hashimi, B. and Nicolici, N, “Synchronization overhead in SoC compressed test”, IEEE Transactions on VLSI Systems, 13(1):pp. 140-153. Jan.05
9. Schmitz, T., Al-Hashimi, B. and Eles, P., “Co-synthesis of energy efficient multimode systems with consideration of mode execution probabilities”, **IEEE Transactions on CAD**, 24(2), pp. 153-170, Feb.05

10. Jafaripناه, M., Al-Hashimi, B. and White, N. M., "Application of Analog Adaptive Filters for Dynamic Sensor Compensation", **IEEE Transaction on Instrumentation and Measurement**, 54(1) pp. 245-251, Apr.05
11. Wilcock, R. Al-Hashimi, B.M., Wilson, P., "Integrated high bandwidth wave elliptic lowpass switched-current filter in digital CMOS technology", **IEE Electronics Letters**, 41(5), pp.222-224, Mar.05
12. Andrei A., Schmitz, M, Eles, P. Peng, Z., Al-Hashimi, B.M., "Overhead-conscious voltage selection for dynamic and leakage energy reduction of time-constrained systems", **IEE Proceedings: Computers & Digital Techniques**, 152(1), pp.28-38, Jan.05
13. Gonciari, P. Al-Hashimi, B., Nicolici, N, "Compression Consideration in Test Access Mechanism Design", **IEE Proceedings: Computers & Digital Techniques**, 152(1),pp. 89-96, 2005
14. Schmitz, M. T., Al-Hashimi, B. M. and Eles, P. "Iterative Schedule Optimisation for Voltage Scalable Distributed Embedded Systems", **ACM Transactions on Embedded Computing Systems**, 3(1) pp. 1-36, Feb.04
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17. Rosinger, P., Al-Hashimi, B. and Nicolici, N. "Scan architecture with mutually exclusive scan segment for shift and capture power reduction", **IEEE Transactions on CAD**, 23(7):pp.1142-1153, Oct.04
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25. Nicolici, N., Al-Hashimi, B.M., "Scan latch partitioning into multiple scan chains for power minimization in full scan sequential circuits", **IEEE Transaction on Computers**, Vol.51, No.6, pp. 721-735, Jun.02
26. Schmitz, M., Al-Hashimi, B.M, Eles, P. "Synthesizing Energy-Efficient Embedded Systems with LOPOCOS", **Design Automation for Embedded Systems**, Vol.6, pp.401-424, 2002
27. Al-Hashimi, B.M, Y. Xie, "Non ideal performance of Bruton transformations switched current wave filters", **IEE Proceedings: Circuits, Systems, and Devices**, 150(1), pp. 6-15, Feb.03
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45. B.M, Al-Hashimi, “Current mode filter structure based on dual output transconductance amplifiers”. **IEE Electronics Letters**, Vol.32,1,25-26, 1996
46. L.F. Lind, B. M. Al-Hashimi and W.P. Somerset, “Linear programming design of FIR raised cosine filters with >100% excess bandwidth”. **IEE Electronics Letters**, Vol.32,5,436-437, 1996
47. B.M.AL-Hashimi, “Understand the fundamental of passive video filters”. **Microwave and RF Journal**, Vol.35, p.171-78, 1996

#### **Refereed Conferences (recent)**

I have published over 120 referred conference papers; a list of selected papers from my most recent publications is provided. For full list, please see <https://ecs.soton.ac.uk/~bmah>

1. Dilillo, L., Rosinger, P., Al-Hashimi, B. M. Girard, P, “Minimizing Test Power in SRAM through Reduction of Pre-charge Activity”. In Proceedings of **DATE 06**



2. Wu, D., Al-Hashimi, B. M. and Schmitz, M. T., Improving Routing Efficiency for Network-on-Chip through Contention-Aware Input Selection. In Proceedings of **ASP-DAC 2006**
3. Cai, Y., Schmitz, M., Ejlali, A., Al-Hashimi, B. and Reddy, S., "Cache Size Selection for Performance, Energy and Reliability of Time-Constrained Systems" In Proceedings of **ASP-DAC 2006**
4. Zhang, Z., M. Reddy, S., Pomeranz, I., Rajski, J. and M. Al-Hashimi, B., "Enhancing Delay Fault Coverage through Low Power Segmented Scan", In Proceedings of **ETS2006**
5. Collins, M. and Al-Hashimi, B. M., "On-Chip Time Measurement Architecture with Femtosecond Timing Resolution", In Proceedings of **ETS2006**
6. Andrei, A., Schmitz, M. T., Eles, P., Peng, Z. and Al-Hashimi, B. M., "Quasi-Static Voltage Scaling for Energy Minimization with Time Constraints". In Proceedings of **DATE 05**
7. Ejlali, A., Schmitz, M., Al-Hashimi, B. M., Miremadi, S. G., "Energy Efficient SEU-Tolerance in DVS-Enabled Real-Time Systems through Information Redundancy". In Proceedings of **ISLPED05**
8. Rosinger, P., Al-Hashimi, B. and Chakrabarty, K., "Rapid generation of thermal-safe test schedules". In Proceedings of **DATE 05**
9. Merrett, G., Al-Hashimi, B. M., White, N. M. and Harris, N. R., "Information Managed Wireless Sensor Networks with Energy Aware Nodes". In Proceedings **NanoTech 2005**
10. Ogg, S. and Al-Hashimi, B., "Improved Data Compression for Serial Interconnected Network on Chip through Unused Significant Bit Removal". In Proceedings of **VLSI Design 05**
11. Andrei, A., Schmitz, M. T., Eles, P., Peng, Z. and Al-Hashimi, B. M. "Overhead-Conscious Voltage Selection for Dynamic and Leakage Power Reduction of Time-Constraint Systems". In Proceedings of **DATE2004**.
12. Andrei, A., Schmitz, M., Eles, P., Peng, Z. and Al-Hashimi, B. M., "Simultaneous Communication and Processor Voltage Scaling for Dynamic and Leakage Energy Reduction in Time-Constrained Systems". In Proceedings of **ICCAD2004**
13. Gonciari, P. T., Al-Hashimi, B.M., "Compression-driven test access mechanism design approach", In Proceedings of **ETS2004** (Best paper award nomination)
14. Wu, D., Al-Hashimi, B. M. and Eles, P., "Scheduling and Mapping of Conditional Task Graphs for the Synthesis of Low Power Embedded Systems". In Proceedings of **DATE 03** (Best paper award nomination)
15. Gonciari, P. T., Al-Hashimi, B. and Nicolici, N., "Useless Memory Allocation: Problems and Solutions". In Proceedings of **VTS 2002**
16. Gonciari, P. T., Al-Hashimi, B. and Nicolici, N., "Integrated Test Data Decompression and Core Wrapper Design for Low-Cost System-on-a-Chip Testing". In Proceedings of **ITC2002**
17. N. Nicolici, Al-Hashimi, B.M., "Power conscious test synthesis and scheduling for BIST RTL data paths". Proceedings of Proceedings of **ITC2000** (Best award paper)

For full details of grant, <http://gow.epsrc.ac.uk/ViewPerson.aspx?PersonId=50450>

## Research Grants

| DATES                 | AWARD HOLDER | FUNDING BODY                                       | TITLE   | VALUE    |
|-----------------------|--------------|--|---|----------|
| July 07-<br>June 2011 | Al-Hashimi*  | EPSRC  | Electronics Design  | £1,006,4 |
| Sep. 06-<br>Aug. 08   | Al-Hashimi*  | EPSRC with ARM<br>(industrial partner)             | Reliable low power<br>embedded<br>computing systems               | £240,447 |
| Mar. 05-<br>Feb. 08   | Al-Hashimi*  | EPSRC, with BAE<br>Systems (industrial<br>partner) | Next generation of<br>interconnection<br>technology for<br>MPSoCs | £260,473 |
| Oct.05-<br>Jul.06     | Al-Hashimi*  | EPSRC  | Support for the 11th<br>IEEE ETS                                  | £15,958  |
| Sept.05-<br>Aug.07    | Al-Hashimi*  | ARM  | PhD studentship   | £39,500  |

|                   |   |  |   |          |
|-------------------|---|--|---|----------|
| Jun.06-<br>May.09 | White*, Harris, Chappel,<br>De Roue, Al-Hashimi | EPSRC<br>(platform grant)                                    | New directions for<br>smart sensors             | £486,869 |
| Jul.04-<br>Jul.07 | Al-Hashimi*                                     | EPSRC/ Philips<br>(Platform grant)                           | Soc design methods<br>and tools                 | £471,590 |
| 2003-2005         | Al-Hashimi*                                     | EPSRC  | Test resource<br>partitioning                   | £209,211 |
| 2003-2005         | Al-Hashimi*                                     | EU FP6   | FIT SoC   | £55,500  |
| 2003-2005         | Al-Hashimi*                                     | EU FP6   | Low power SoC                                   | £55,500  |
| 2002-2005         | Al-Hashimi*,                                    | EPSRC  | Low power BIST                                  | £165,320 |
| 2000-2003         | Al-Hashimi*                                     | EPSRC  | SI filters and<br>equalizers                    | £158,487 |
| 1997-1999         | Al-Hashimi*                                     | Fujitsu<br>Microelectronics                                  | HLS with testability                            | £16,000  |
| 1996-1999         | Al-Hashimi*                                     | EPSRC/Industrial case<br>studentship<br>(Faraday Technology) | Mixed signal circuit<br>design                  | £45,000  |
| 1996-1998         | Al-Hashimi*                                     | Faraday Technology   | CMOS video filters                              | £45,000  |
| 1996-1998         | Al-Hashimi*                                     | WML Ltd  | Analog FPGA                                     | £14,000  |
| 1996              | Al-Hashimi*                                     | EPSRC  | Digital system<br>design (MSc IGDS<br>course)   | £22,000  |
| 1995-1997         | Al-Hashimi*                                     | Faraday Technology   | FPGA complier for<br>DSP                        | £45,000  |
| 1995-1997         | Al-Hashimi*                                     | Nuffield Foundation  | Raised cosine<br>filtering for digital<br>video | £30,000  |

\* Principal Investigator

## Recent Professional Activities

I have always maintained a high international profile within my general subject area. Recent examples:

- IEEE European Test Symposium, General Chair, Southampton, May.06, Executive Committee Member
- DATE Friday Workshops, General Chair, 05, 06 and 07, Executive Committee Member
- DATE Conference, Technical Program Vice-Chair (2008), Technical Program Chair (2009)
- IEE Professional Network (Embedded Microelectronics Systems”, Executive Committee Member
- IEE EDA Tools Forum, co-chair with Prof. P. Cheung (Imperial College), London, Nov.04
- IEE Colloquium “Hardware-Software Co-design”, Chair, December 2000
- External Examiner at
  - York University, BEng/MEng Electronics Eng., Oct. 04- present
  - University of Glasgow, MSc Electronics and Electrical Eng., Jan. 06- present

## Recent Invited Talk

I had numerous invited presentations to report on our research findings. Recent examples:

- Keynote address, "Energy Management and Fault Tolerance in Real-Time Embedded Systems”, 20th Conference on Design of Circuits and Integrated Systems, Portugal, Nov.05
- Low Power System Level Design, ARM (Cambridge), Jun.05
- Compression Based Manufacturing Test, Mentor Graphics, UK (Swindon), Apr.04
- Power Constrained Testing of VLSI Chips, Philips Semiconductor, Southampton, Sep.03
- SoC Manufacturing Test: A Personal Perspective, IEE Seminar on System on Chip Design Challenges, London, Nov.02