COE 571 Digital System Testing
Term 072

<u>List of Paper Presentations</u>:

1. W. Zou, W.-T. Cheng, S. M. Reddy and H. Tang, "Speeding Up Effect-Cause Defect Diagnosis Using a Small Dictionary", in Proc. VLSI Test Symp., 2007, Paper 6B-2.

2. B. Seshadri, I. Pomeranz, S. Venkataraman and S.M. Reddy, “Dominance Based analysis for Large Volume Production Fail Diagnosis”, in Proc. VTS 2006, pp. 392-399.

3. D. B. Lavo I. Hartanto, and T. Larrabee, " Multiplets, Models, and the Search for Meaning: Improving Per-Test Fault Diagnosis", in Proc. ITC, 2002, pp. 250-259.

4. P. Bernardi, M. Grosso, M. Rebaudengo and M. Sonza Reorda, "A Pattern Ordering Algorithm for Reducing the Size of Fault Dictionaries", in Proc. VLSI Test Symposium, Apr. 2006, pp. 386-391.

5. T. Bartenstein, D. Heaberlin, L. Huisman and D. Sliwinski, "Diagnosing Combinational Logic Designs Using the Single Location At-A-Time (SLAT) Paradigm", in Proc. Intl. Test Conf., 2001, pp. 287-296.

6. Z. Wang, M. M. Sadowska, et al., "An Efficient and Effective Methodology on the Multiple Fault Diagnosis", in Proc. ITC, 2003, pp. 329-338.

7. L.M. Huisman, M. Kassab and L. Pastel, “Data mining integrated circuit fails with fail commonalities”, Proc. Intl. Test Conf., 2004, pp. 661 – 668.

8. C. Hora, R. Segers, S. Eichenberger and M. Lousberg, “An effective diagnosis method to support yield improvement”, Proc. Intl. Test Conf., 2004, pp. 260-269.